WiNRADiO®

WR-G65DDCe
Multichannel Coherent Application Guide

Version 1.03

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1 Introduction

The WiNRADiO WR-G65DDCe receiver optionally provides multichannel coherent operation. A minimum of two and up to sixteen receivers can be coupled together for multichannel operation. By cascading the devices, it is possible to couple more (tens or even hundreds of receivers).

The receivers have to be connected to the PC through their USB3 interface. The LAN interface is not supported in the coherent mode.

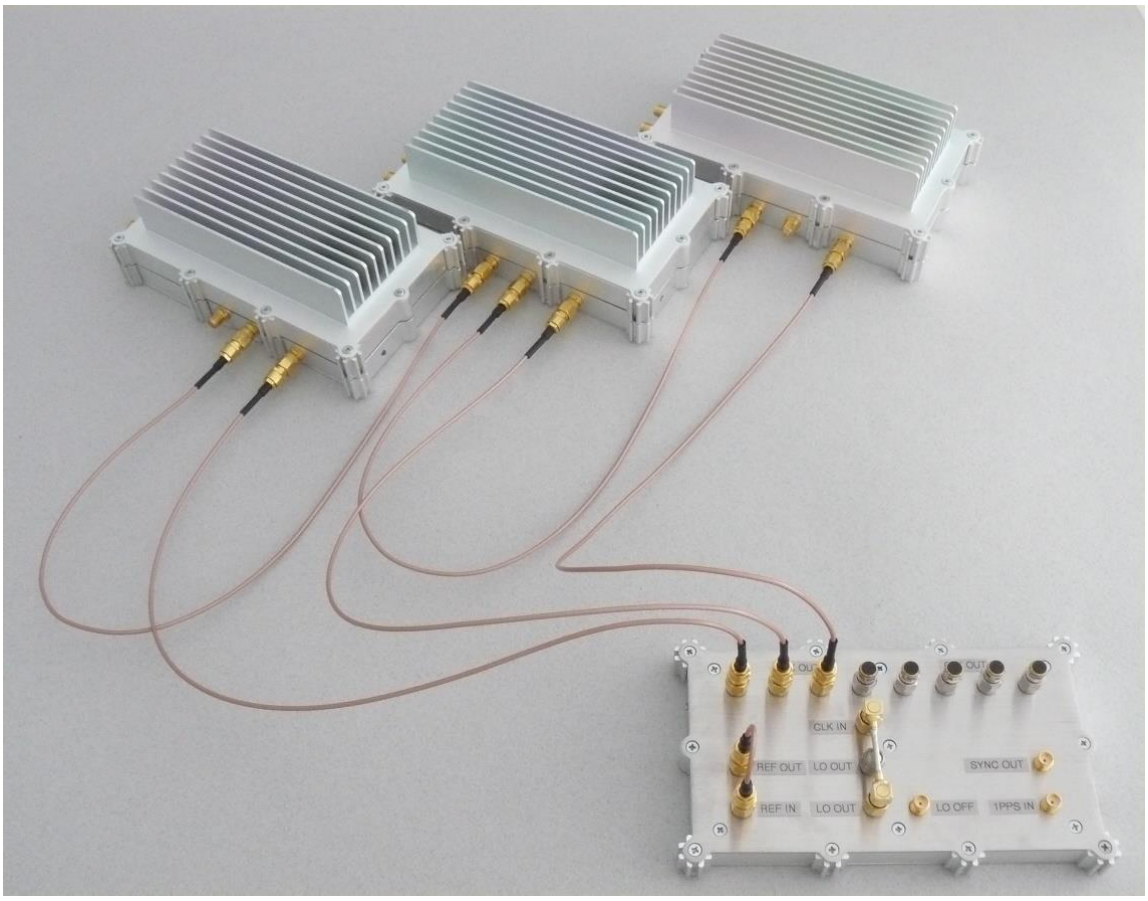
There are two topologically distinct ways in which the coherent receivers can be connected to the PC over their USB3 interface. The first way is the standard installation, where all coherent receivers are connected to the same PC, which allows for centralized processing of coherent signals. The second way is the Extended Topology Configuration (ETC), where each receiver is connected to a separate dedicated PC. This allows for implementation of advanced parallel computing algorithms for phase-coherent systems. For more information on the Extended Topology Configuration (ETC) please refer to Chapter 5 of this document.

To couple up to eight receivers, the **WR-CC1PPS-210e** 'WiNRADiO WR-G65DDCe Coherence Clock & 1PPS Kit' has to be used, which is described in the Section 2.2. To couple from nine to sixteen receivers, two Kits have to be used. For more than sixteen channels please contact WiNRADiO.

For coherent operation, all WR-G65DDCe receivers must be clocked at exactly the same frequency and phase. To achieve this requirement, it is necessary to distribute a sampling clock from a single low phase noise clock source. Therefore, **the receivers have to be equipped with a coherent receiver option (/CR)** for external sampling clock provision.

Similar to the sampling clock, all commands and operations of the receivers must be synchronized accordingly to the coherent sampling clock. For this reason the receivers have an external interconnection for digital synchronization, which is also provided on receivers with a coherent receiver option (/CR).

An example of a coherent three channel system is shown in Picture 1-2.



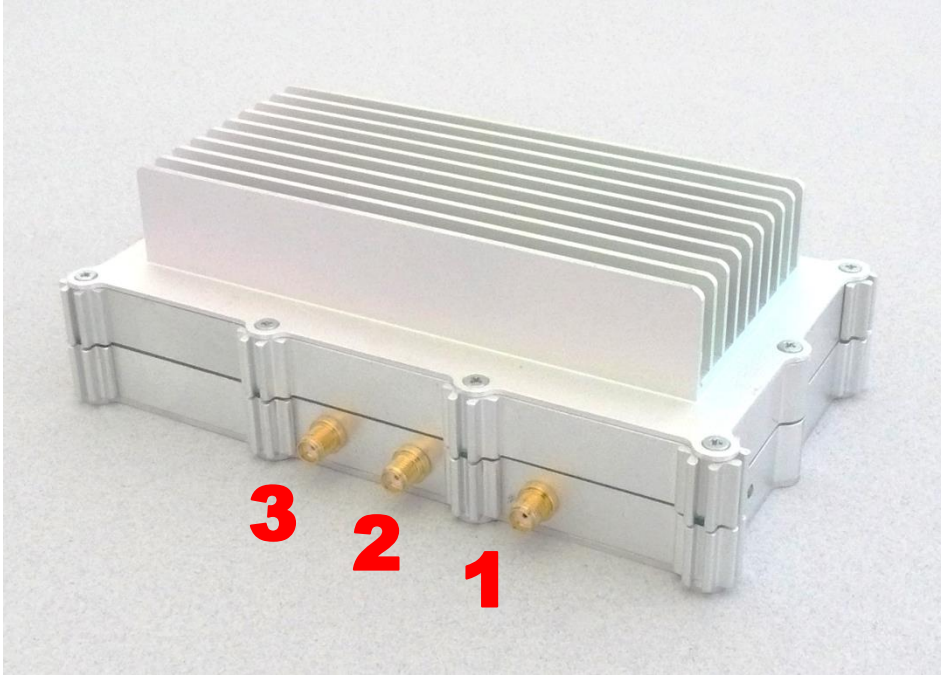
Picture 1-2: An example of three WR-G65DDCe receivers in coherent configuration

2 Parts description of the coherent system

2.1 WR-G65DDCe connectors

The connectors required for coherent operation of the WR-G65DDCe receivers are shown in Picture 2-1 (present when the /CR option has been fitted):

1. **CLK IN** – ADC clock input
2. **SYNC IN** – digital synchronization input
3. **SYNC OUT** – digital synchronization output

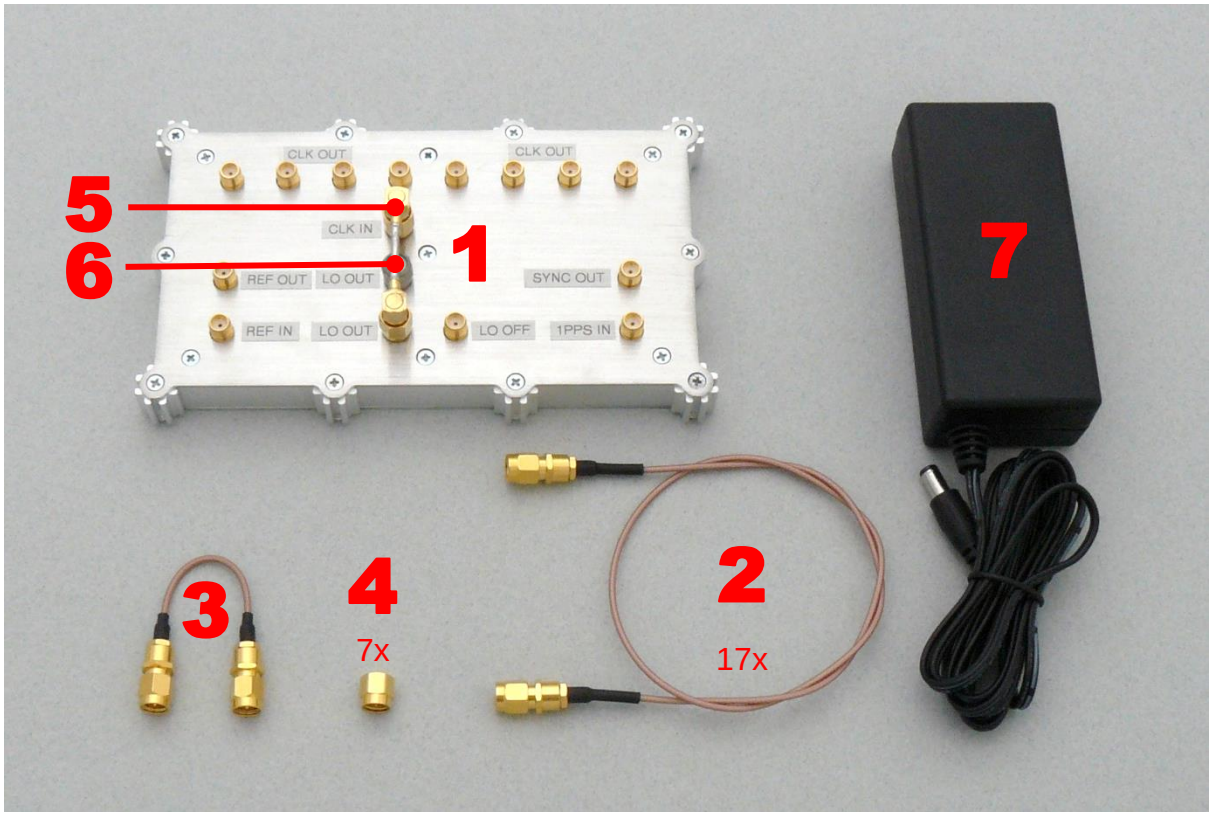


Picture 2-1: The connectors required for coherent operation of the WR-G65DDCe

2.2 The WiNRADiO Coherence Clock & 1PPS Kit (WR-CC1PPS-210e)

The 'WiNRADiO Coherence Clock & 1PPS Kit' (hereafter referred to as the '**Kit**') provides production and distribution of a coherent 210 MHz clock for up to eight WR-G65DDCe receivers as well as digital synchronization of the receivers. It also features an internal frequency reference of 0.1 ppm stability, input for external frequency reference and digital input for a 1PPS pulse. The Kit consists of the following components (shown in Picture 2-3):

1. Coherent clock generator unit with 1PPS input
2. SMA patch cables for coherent clock distribution and synchronization (17 pcs)
3. Frequency reference SMA interconnect cable
4. SMA terminators (7 pcs + 1 piece pre-installed on the unit, see 6 below)
5. Sampling clock SMA coaxial jumper (factory pre-installed on the unit)
6. Sampling clock SMA terminator (factory pre-installed on the unit)
7. Power adapter



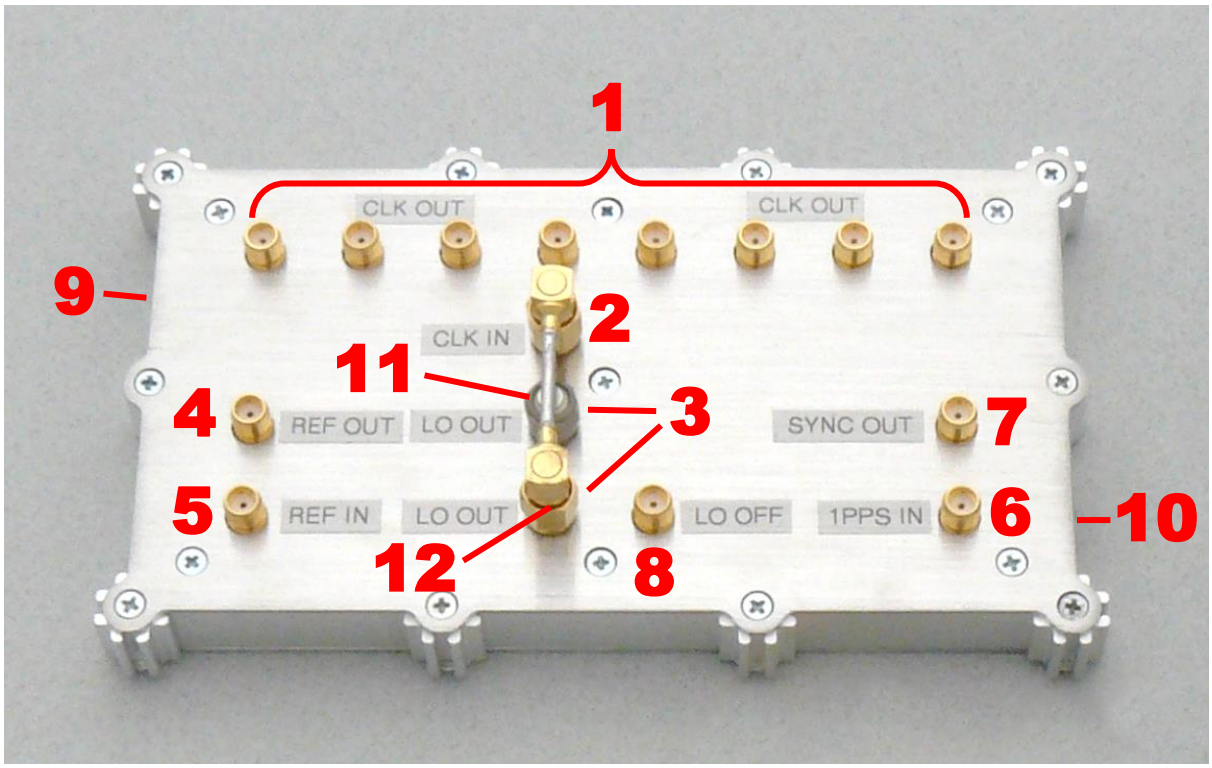
Picture 2-2: The WiNRADiO WR-G65DDCe Coherence Clock & 1PPS Kit

2.2.1.1 Coherent clock generator unit with 1PPS input

The coherent clock generator unit (hereafter referred to as the '**Unit**') is shown in Picture 2-3. It is a standalone device, which has to be installed next to and connected to the WR-G65DDCe receivers thus creating the coherent group of receivers. The unit generates a 210 MHz sampling clock for up to eight WR-G65DDCe receivers. The sampling clock is locked to a frequency reference, which can be internal or external. It also distributes a 1PPS trigger signal from the 1PPS input to all connected WR-G65DDCe receivers via the digital synchronization interface port SYNC OUT.

No software driver is required for operation of the Coherent clock generator unit.

For the technical specification of the unit, please refer to Chapter 6 of this document.



1 Sampling clock outputs LO OUT
2 Local oscillator input LO IN
3 Local oscillator output LO OUT
4 Frequency reference output REF OUT
5 Frequency reference input REF IN
6 1PPS input 1PPS IN
7 Synchronization signal output SYNC OUT
8 LO OFF connector for disabling of the internal oscillators
9 Power / Locked indicator (front panel)
10 Power supply connector (back panel)
11 Factory pre-installed SMA terminator
12 Factory pre-installed SMA jumper

Picture 2-3: Front view of Coherent clock generator unit

2.2.1.2 CLK OUT connectors for sampling clock output

There are eight SMA connectors for the sampling clock output provided on the Coherent clock generator unit. These are located on the top of the unit and are facing upwards. The CLK IN input of each WR-G65DDCe receiver within a coherent group must be connected to one of these ports using the SMA patch cables (for coherent clock distribution) supplied with the Kit and described in Section 2.2.2. All ports are equivalent; therefore, any receiver within a coherent group can be connected to any of these ports. However, unused ports have to be terminated using the 50 ohm SMA terminators for proper operation.

For the technical specification of the sampling clock output signal, please refer to Chapter 6.

2.2.1.3 Sampling clock oscillator input CLK IN

The CLK IN port drives all eight CLK OUT outputs. In other words, the sampling clock provided at this port is coherently distributed to all eight CLK OUT outputs, therefore it must always be connected to one of the two LO OUT output ports described in the next section. This mandatory connection is factory installed as shown in Picture 2-10 and described in Section 2.2.5.

The factory connection between the LO OUT port and the CLK IN port should not be altered for normal operation when using the coherent clock generator unit to drive up to eight coherent receivers.

The purpose of this connection is to enable the use of **two coherent clock generator units** to coherently drive up to sixteen receivers. For details on how to use two coherent clock generator units to drive up to sixteen receivers please refer to chapter 4 of this document.

2.2.1.4 Sampling clock oscillator outputs LO OUT

There are two LO OUT ports provided on the Unit. Both LO OUT ports provide the same phase coherent 210 MHz sampling clock signal generated by the internal sampling clock oscillator.

The purpose of the two LO OUT ports is to enable the use of **two coherent clock generator units** to coherently drive up to **sixteen receivers**. For details on how to use two coherent clock generator units to drive up to sixteen receivers please refer to chapter 4 of this document.

For the standard operation of a **single Coherent clock generator** unit driving up to **eight receivers**, one of these ports has to be connected to the CLK IN port on the unit. The other one has to be terminated using a 50 ohm SMA terminator.

This mandatory connection between the LO OUT port and the CLK IN port is factory installed as shown in Picture 2-10 and described in Section 2.2.5. It consists of a SMA jumper cable connecting the LO OUT port and the CLK IN port. This interconnects the sampling clock from the sampling clock oscillator output LO OUT to the CLK IN input of the Coherent clock generator unit. The other unused LO OUT port is terminated using a 50 ohm terminator.

The factory connection between the LO OUT port and the CLK IN port should not to be altered for normal operation when using the coherent clock generator unit to drive up to eight coherent receivers.

For details on how to use two coherent clock generator units to drive up to sixteen receivers please refer to Chapter 4 of this document.

2.2.1.5 Frequency reference output REF OUT

The frequency reference output is an SMA connector providing the 10 MHz (internal) frequency reference output signal. This output can be connected to the REF IN input port (Section 2.2.5) if the internal frequency reference operation of the Unit is required. Use the Frequency Reference SMA Interconnect cable (described in Section 2.2.3 and provided with the Kit) to connect the REF OUT port to the REF IN port.

If unused, this port must be properly terminated using the 50 ohm terminator.

For the technical specification of the REF OUT, please refer to Chapter 6.

2.2.1.6 Frequency reference input REF IN

A signal provided to the frequency reference input REF IN serves as a frequency reference for the internal 210 MHz sampling clock generator, thus providing the frequency reference for whole coherent system. The connection is via a 50 ohm terminated SMA connector. A 10 MHz reference signal must be provided on this input.

This input can be connected to the REF OUT output port (Section 2.2.4) if the internal frequency reference operation of the unit is required. Use the Frequency Reference SMA Interconnect cable (described in Section 2.2.3 and provided with the Kit) to connect the REF OUT port to REF IN port.

For the technical specification of the REF IN input, please refer to Chapter 6.

2.2.1.7 1PPS IN input

The 1PPS IN input is provided for applications which require external synchronization (using a 1PPS signal from a GPS or similar source). The connection is via a 50 ohm terminated SMA connector, which accepts 5V TTL logic levels.

The signal provided to this input is processed by a fast logic comparator and then distributed to all of the receivers within a coherent group of receivers - over the Digital synchronization output SYNC OUT described in next Section. If the 1PPS IN input is used, the SYNC OUT has to be connected as well as described in Section 3.4.

Please note that, the 1PPS signal is not needed for coherent operation of the WR-G65DDCe receivers. The only purpose of the 1PPS signal is to provide a time base for the function of

time-stamping. The coherent operation of the receivers is not affected by the 1PPS signal at all. If unused, this port can be left unconnected.

For the technical specification of the input, please refer to Chapter 6.

2.2.1.8 Digital synchronization output SYNC OUT

The digital synchronization output SYNC OUT provides a connection to the digital synchronization interconnection within a coherent group of receivers. Connection is via the SMA patch cables for coherent clock distribution and synchronization (described in Section 2.2.2). It distributes the 1PPS signal from the 1PPS IN input of the Coherent clock generator unit to all of the WR-G65DDCe receivers within a coherent group.

If the 1PPS IN input is not used, the SYNC OUT can be left unconnected as well.

The synchronization protocol utilized on this interface is proprietary to WiNRADiO therefore no further specification is provided.

2.2.1.9 LO OFF connector for disabling the sampling clock oscillator

Installing the 50 ohm terminator to the LO OFF port turns off all internal oscillators (reference frequency generator and 210 MHz sampling clock oscillator).

This port has to be left open for normal operation of a single coherent clock generator unit, keeping the internal oscillators running normally.

The purpose of the LO OFF port is to provide the ability to turn off the local sampling clock oscillator and the internal frequency reference of the coherent clock generator unit on the slave unit when two coherent clock generator units (master and slave) are used to coherently drive up to sixteen receivers - thus preventing unwanted interference and degraded performance. To turn off the local sampling clock oscillator and internal frequency reference, install a 50 ohm terminator to this port. For details on how to use two coherent clock generator units to drive up to sixteen receivers please refer to chapter 4 of this document.

2.2.1.10 Power / Locked indicator

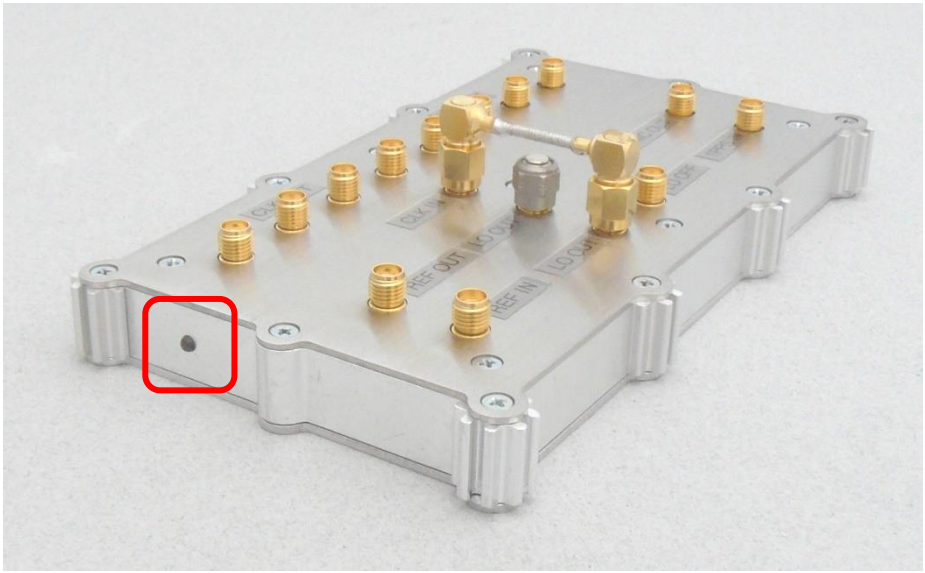
The Power / Locked indicator is the blue color LED located on the front panel of the Coherent clock generator unit as shown in the Picture 2-4. It indicates whether the unit is powered as well as indicating the state of the internal oscillators. Four states are indicated: no power, PLL locked, PLL not locked and internal oscillators turned off.

LED off indicates that the device has **no power**.

LED steady on, pulsing briefly every 4 seconds indicates that the **PLL is locked**, i.e. the 210 MHz sampling clock generator is locked to the frequency reference signal provided at the REF IN port. This is the normal state of operation. For more information about the REF IN port please refer to Sections 2.2.1.6 and 3.3.

LED flashing quickly indicates that the internal **PLL is NOT locked**, i.e. the frequency reference signal is not present at the REF IN port, or the frequency reference signal doesn't meet the required specification. For the technical specification of the frequency reference signal please refer to Chapter 6.

LED steady on indicates that **the internal oscillators are turned off**, i.e. the 50 ohm terminator is installed on the LO OFF port. For details, please refer to Section 2.2.1.9 and 4.1.



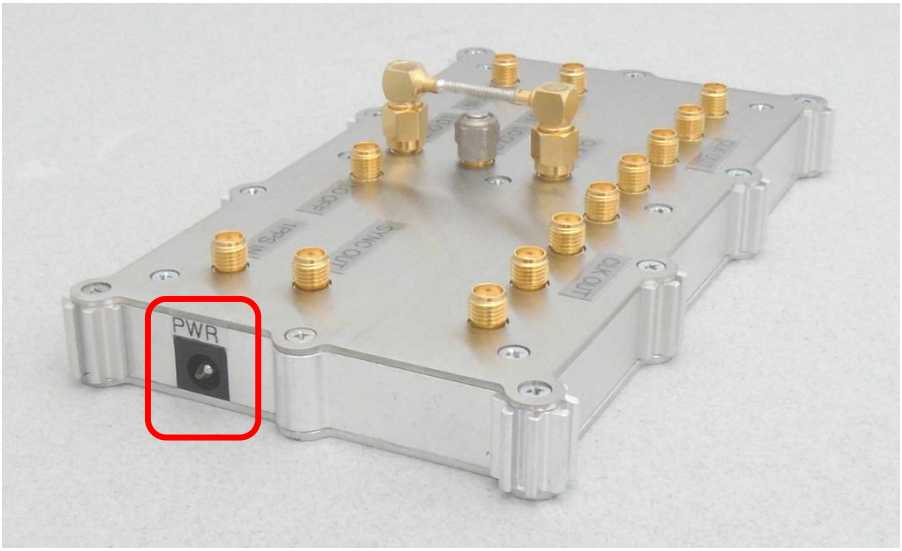
Picture 2-4: The Power / Locked indicator LED located on the front panel marked in red

2.2.1.11 Power input socket

The power input socket provides power to the Coherent clock generator unit. It is located on the back panel of the coherent clock generator unit as shown in the Picture 2-5. The power adapter supplied with the Kit connects to this socket.

For the technical specification of the power requirements, please refer to Chapter 6.

CAUTION: *For best performance and safety, we recommend using only the power adapter supplied by WiNRADiO, which comes included with your Coherent clock generator unit.*



Picture 2-5: The Power input socket of the Coherence clock generator unit located on the back panel, marked in red

2.2.2 SMA patch cables for coherent clock distribution and digital synchronization

There are seventeen SMA patch cables supplied with the Kit.

Eight of these SMA patch cables are used to distribute the sampling clock from the Coherent clock generator unit to all of the WR-G65DDCe receivers which are in coherent operation as described in Section 3.1.

Another eight SMA patch cables are used to synchronize all commands and operations of the WR-G65DDCe receivers within a coherent group. A single SMA patch cable is needed for each WR-G65DDCe receiver. The synchronization connection is made in a daisy-chain manner, always linking the SYNC OUT of the previous receiver with the SYNC IN of the next receiver in the chain as described in Section 3.2.

The seventeenth cable is used when two kits are connected together to drive up to 16 receivers as described in Chapter 4.

For interconnection, only use the original WiNRADiO SMA patch cables supplied with the Kit as these are specially matched to be coherent.

Picture 2-6: WiNRADiO coherent SMA patch cable

2.2.3 Frequency reference SMA interconnect cable

The frequency reference SMA interconnect cable is used to interconnect the internal reference output REF OUT of the Coherent clock generator unit to the frequency reference input REF IN of the same unit when the internal reference frequency operation is required. If an external frequency reference is used, this cable is not needed and should be kept safely, in case the internal reference operation is required in the future.

For installation of the cable please refer to Section 3.3 of this document.

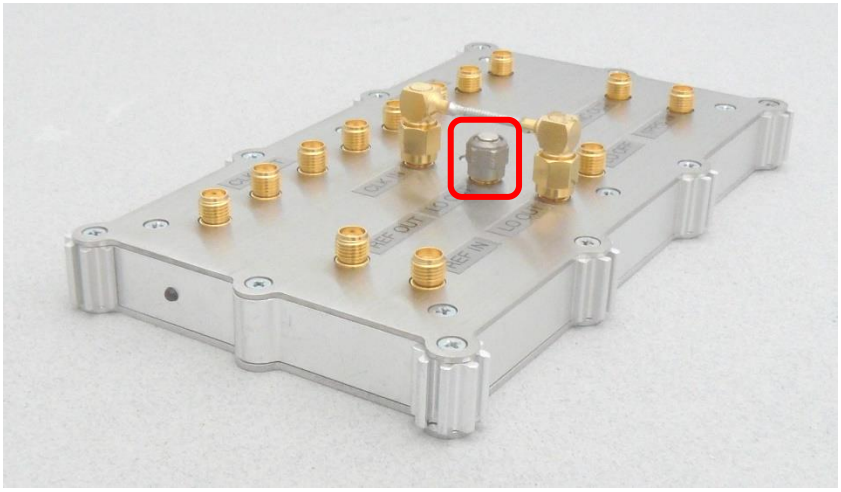
Picture 2-7: SMA interconnect cable for frequency reference

2.2.4 SMA terminators

The Kit comes with eight 50 ohm SMA terminators. These terminators must occupy all unused sampling clock outputs on the Coherent clock generator unit. A minimum of two WR-G65DDCe receivers can be connected as a coherent pair, so six terminators are needed to terminate the sampling clock outputs. The seventh terminator is provided in case the external reference is used with the Coherent clock generator unit. In such a case, the terminator must be installed on the REF OUT port of the Coherent clock generator unit.

Picture 2-8: SMA terminators

The eighth terminator comes factory pre-installed on the Coherent clock generator unit, terminating the secondary sampling clock oscillator output as shown in picture 2-9.



Picture 2-9: SMA terminator (marked in red) factory pre-installed on the secondary sampling clock oscillator output

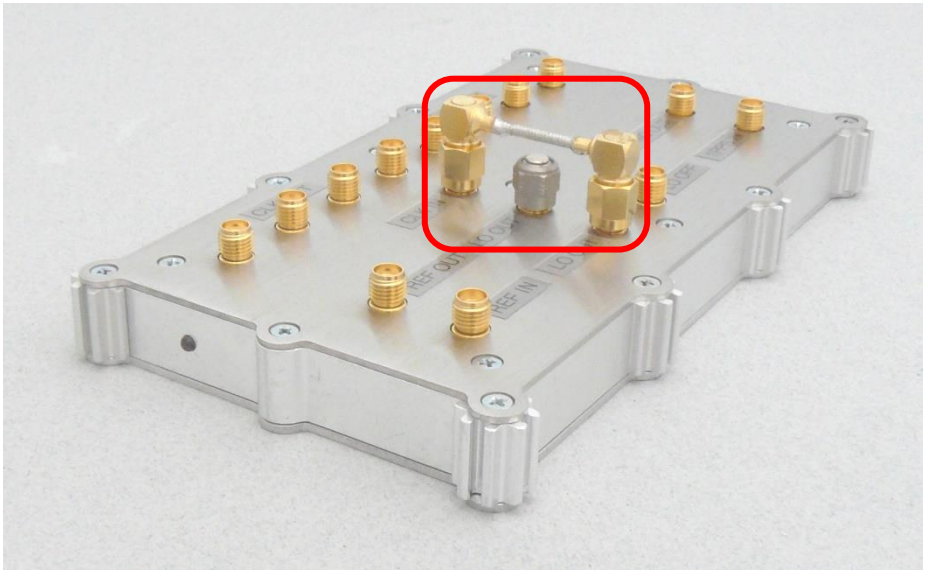
2.2.5 SMA jumper cable and the factory pre-installed LO OUT to CLK IN interconnection

The Kit comes with an SMA jumper cable used to connect the primary sampling clock oscillator output LO OUT to the sampling clock oscillator input CLK IN.

This SMA jumper is factory pre-installed connecting the LO OUT port with the CLK IN port as shown in picture 2-10. Also, the mandatory 50 ohm terminator is factory pre-installed on the other unused LO OUT port.

The factory connection should not to be altered for normal operation when using the coherent clock generator unit to drive up to eight coherent receivers.

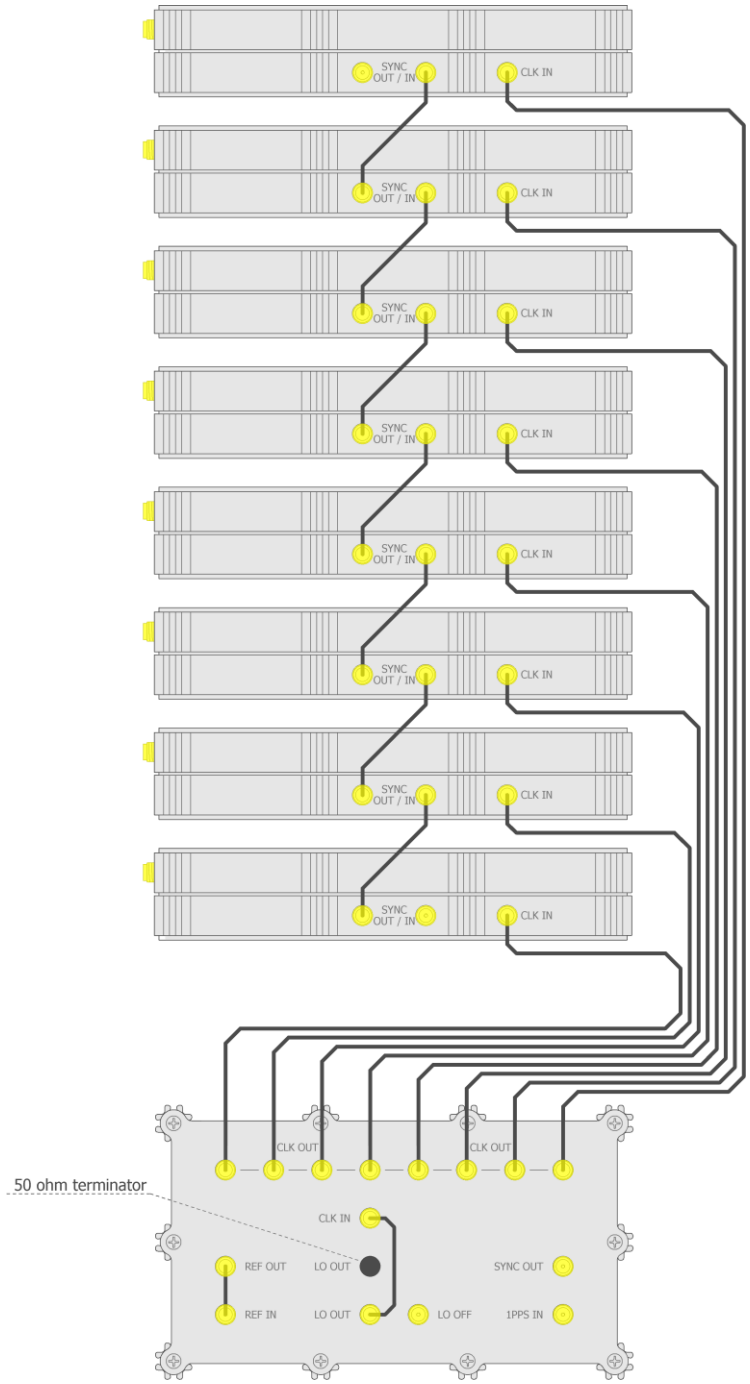
The jumper must be replaced with a proper patch cable when using two Coherent clock generator units to distribute the sampling clock to up to sixteen receivers. For details on how to use two coherent clock generator units to drive up to sixteen receivers please refer to chapter 4 of this document.



Picture 2-10: Factory pre-installed SMA jumper cable (marked in red) interconnecting the LO OUT sampling clock oscillator output with the CLK IN sampling clock oscillator input. Please note the mandatory terminator installed on the other unused LO OUT sampling clock oscillator output

3 Standard installation of up to eight receivers

The basic setup of eight receivers is shown in Picture 3-1. The setup consists of a minimum two and up to eight WR-G65DDCe/CR receivers connected to the PC through the USB3 port. The receivers are interconnected with the Coherent clock generator unit through their CLK IN port and also with each other through their SYNC IN and SYNC OUT ports in a daisy-chain like manner to allow for digital synchronization. The SMA patch cables described in Section 2.2.2 are used for these interconnections.



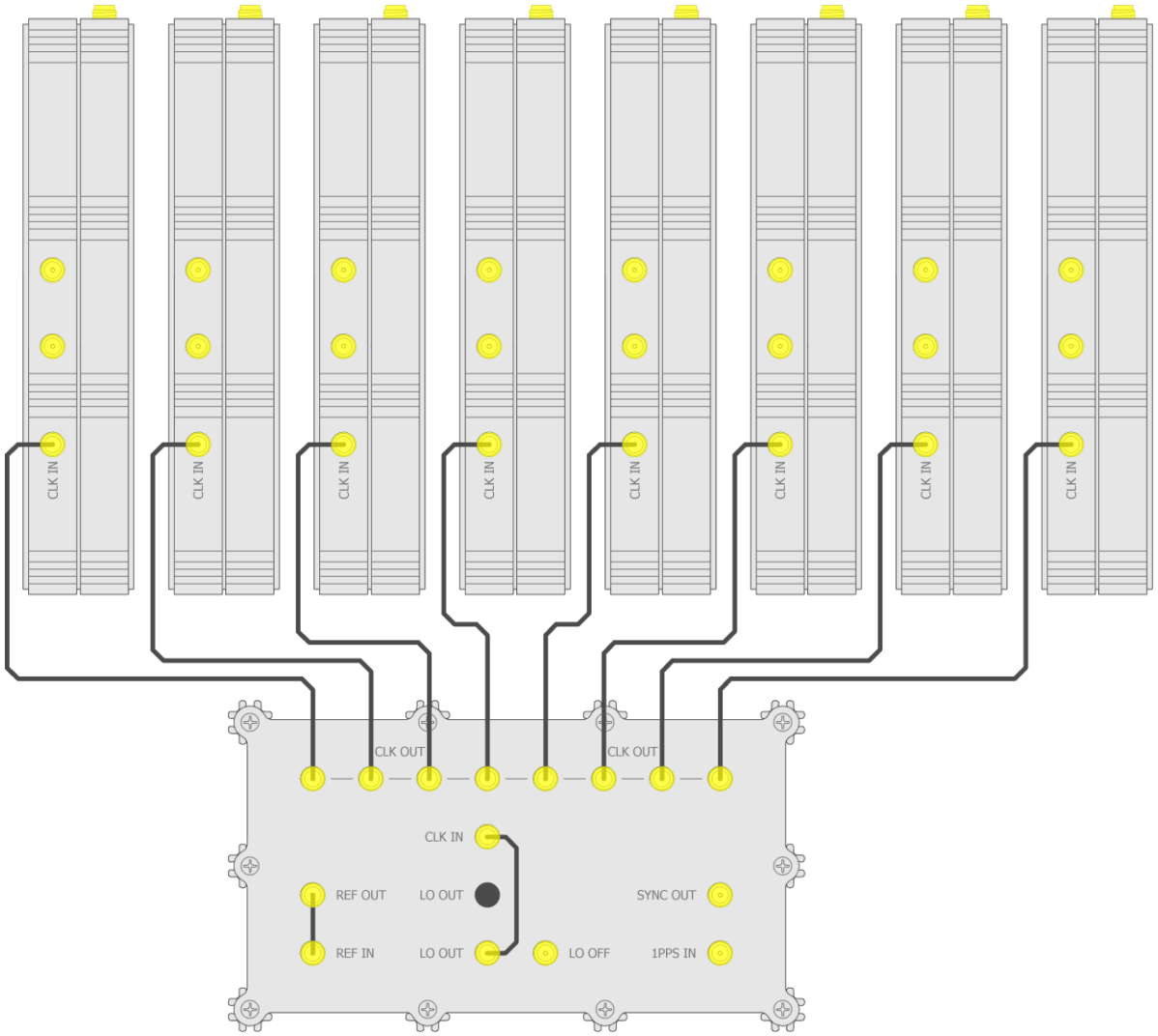
Picture 3-1: Sampling clock and digital sync signal interconnection of eight WR-G65DDCe receivers together with the Coherent clock generator unit

3.1 Connecting the sampling clock interconnection

The sampling clock interconnection is made between the CLK OUT port of the Coherent clock generator unit described in Section 2.2.1.1 and the CLK IN port of each receiver described in Section 2.1.

The SMA patch cables described in Section 2.2.2 must be used for the sampling clock interconnection. All cables used for clock distribution must be of the same type and length. Cables of various types and lengths cannot be used within one coherent group of receivers. For interconnection, only use the original WiNRADiO SMA patch cables supplied with the Clock Kit as these are specially matched to be coherent.

The connection is made in a star-like manner, always linking one of the CLK OUT port of the Coherent clock generator unit with one CLK IN port of the as shown in Picture 3-2.



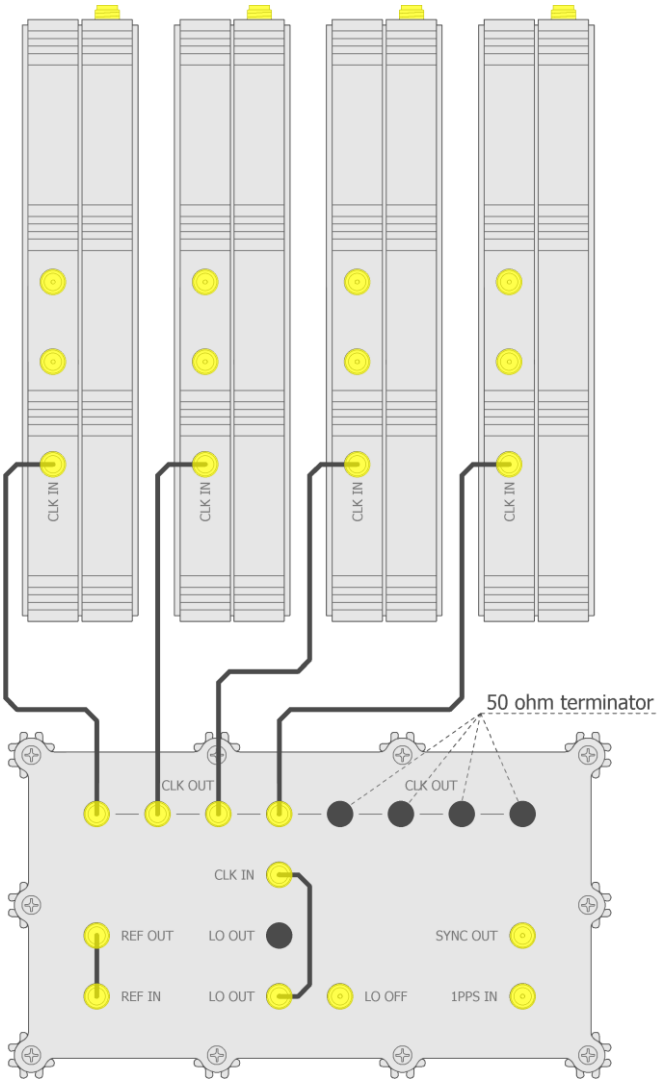
Picture 3-2: Connecting the sampling clock interconnection. The SMA patch cables described in Section 2.2.2 must be used for the interconnection

All receivers within one coherent group are equal from the clock distribution point of view.

The number of the receivers which can be coherently clocked by one Coherent clock generator unit is up to eight. Two units can be linked for driving up to sixteen receivers as described in Chapter 4. If more than sixteen channels are required, please contact WiNRADiO.

Also please note that the sampling clock interconnects in the Picture 3-2 are drawn for clarity and there is no need to connect the sampling clock input CLK IN of any particular receiver to any specific CLK OUT position on the Coherent clock generator unit. Instead; all sampling clock outputs CLK OUT on the Coherent clock generator unit are equivalent.

If any of the ports on the Coherent clock generator unit are unused, all unused ports have to be terminated using the 50 ohm SMA terminators for proper operation (as shown in the Picture 3-3). In this picture only four clock outputs are utilized, while the other four unused ports are terminated using 50 ohm terminators.



Picture 3-3: When connecting the sampling clock interconnection to less than eight receivers, SMA 50 ohm terminators must be installed on any unused clock output ports

3.2 Connecting the SYNC interconnection

The SYNC interconnection is made between the receivers only.

The SMA patch cables described in Section 2.2.2 must be used for the SYNC interconnection.

All cables used for synchronization must be of the same type and length. Cables of various types and lengths cannot be used within one coherent group of receivers. For interconnection, only use the original WiNRADiO SMA patch cables supplied with the Clock Kit as these are specially matched to be coherent.

The connection is made in a daisy-chain manner, always linking SYNC OUT of the previous receiver with the SYNC IN of receiver in the chain (as shown in Picture 3-4).

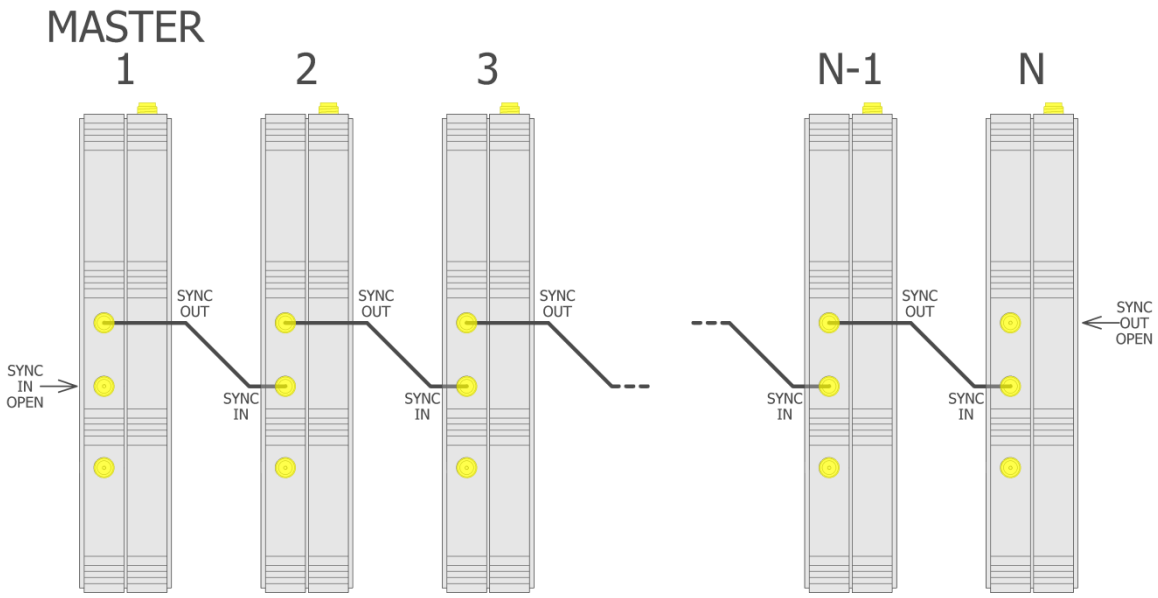
The first receiver in a chain is called the synchronization master and is designated as ‘1’ in the Picture 3-4. The master receiver generates the synchronization signal and sends it down the synchronization chain. Therefore, the SYNC IN connector on the master receiver is left unconnected.

The synchronization signal from the master is received by the receiver second in the synchronization chain designated as ‘2’ in the Picture 3-4. It is received at its SYNC IN input. It is then re-sent through its SYNC OUT output and received by receiver ‘3’ at its SYNC IN input, which also re-sends it through its SYNC OUT to the receiver next in the chain. This way, the synchronization signals propagate down the synchronization chain from receiver-to-receiver, and finally to the receiver which is the last in the chain. The receiver which is the last in chain is designated as ‘N’ and has its SYNC OUT output left open, as there is no other receiver which could receive the synchronization signal.

The number of the receivers which can be synchronized is unlimited in theory, but currently it is limited to 16. If more than sixteen channels are required, please contact WiNRADiO.

Each SMA patch cable delays the synchronization signal by a certain time. The delay value is an integer number, which specifies the amount of sampling clock periods by which the cable delays the signal. The user must specify the delay of the SMA patch cables in the software, so that the software can compensate for the delay. The SMA patch cables supplied with the kit delay the synchronization signal by 1 sampling clock period.

As mentioned above, the SMA patch cables described in Section 2.2.2 must be used for the SYNC interconnection. All SYNC cables used for synchronization must be of the same delay. Cables of various delays cannot be mixed within one coherent group of receivers.



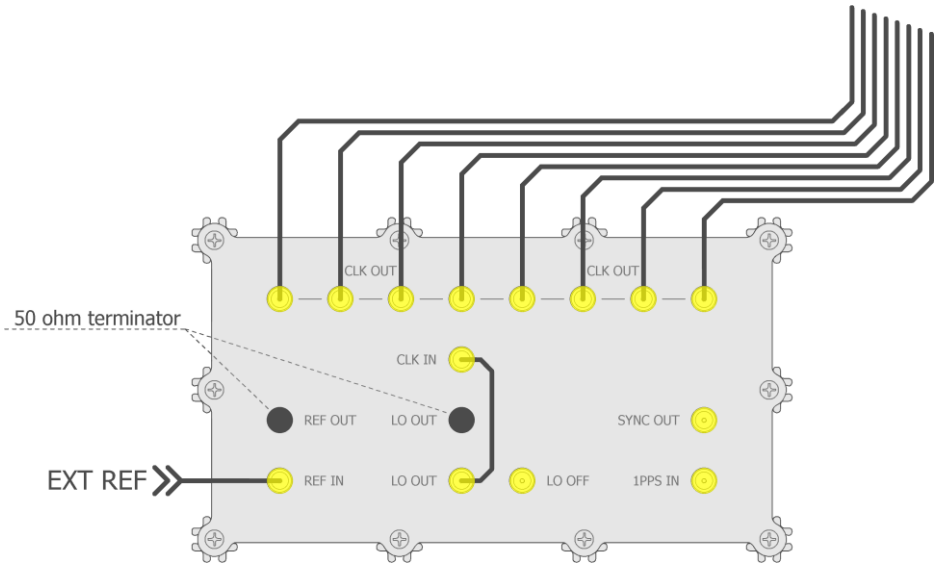
Picture 3-4: The SYNC interconnection is made in a daisy-chain manner, always linking SYNC OUT of the previous receiver with the SYNC IN of next receiver. The SMA patch cables described in Section 2.2.2 must be used for the interconnection. Only the SYNC interconnection is shown in the picture, other interconnections are omitted for clarity

3.3 Choosing the frequency reference

When using the internal frequency reference, please connect the internal reference output REF OUT of the Coherent clock generator unit to the frequency reference input REF IN of the unit as shown in Picture 3-5. Please use the Frequency reference SMA interconnect cable as described in Section 2.2.3.

When using an external frequency reference, please connect the frequency reference signal to the REF IN port of the Coherent clock generator unit as shown in the Picture 3-6 and as described in Section 2.2.1.6. Please note that the REF OUT port has to be properly terminated using a 50 ohm terminator when unused.

Picture 3-5: Installing the frequency reference SMA interconnect cable for internal frequency operation



Picture 3-6: When using the external frequency reference, connect the external frequency reference to the REF IN port and install a 50 ohm terminator on the REF OUT port as well

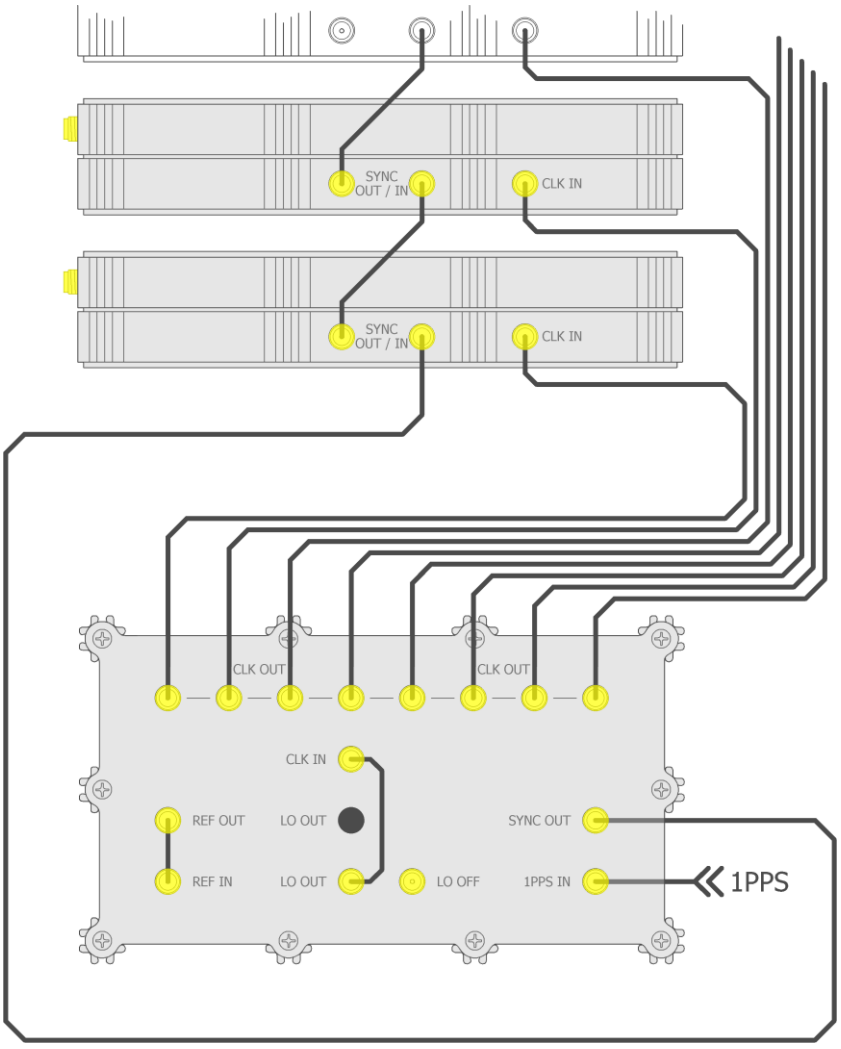
3.4 Using the 1PPS signal

The 1PPS signal is not needed for coherent operation of the WR-G65DDCe receivers. However, if a function of time stamping is required, the user has to provide the 1PPS signal from a GPS receiver or similar timing source.

Connect the 1PPS signal to the 1PPS IN port on the Coherent clock generator unit. In this scenario, use the SMA patch cable described in Section 2.2.2 to connect the SYNC OUT port of the Coherent clock generator unit to the SYNC IN port of the receiver which is connected as the first in the synchronization chain as shown in the Picture 3-7.

If the 1PPS signal is not used, the 1PPS IN port and the SYNC OUT port on the Coherent clock generator unit can be left unconnected.

For the technical specification of the 1PPS IN port requirements for the 1PPS signal, please refer to Chapter 6 of this document.



Picture 3-7: When use of the 1PPS signal is required, connect it to the 1PPS IN port on the Coherent clock generator unit. The SYNC OUT port of the Coherent clock generator unit has to be connected to the SYNC IN port of the receiver which is connected as the first in the synchronization chain as shown here

3.5 Power up of the Coherent clock generator unit

Connect the power adaptor supplied with the Kit (Section 2.2) to the power input socket of the Coherent clock generator unit described in Section 2.2.1.10. The Power / Locked indicator described in Section the Section 2.2.1.9 will light up indicating the presence of power. For details on various states indicated by Power / Locked indicator please refer to Section 2.2.1.9.

CAUTION: *For best performance and safety, we recommend using only the power adapter supplied by WiNRADiO, which comes included with the Coherent clock generator unit.*

3.6 Finishing the installation of the receivers

Finish the installation of the receivers by connecting the power adapter to each receiver and USB3 connection to the PC followed by installation of the device drivers and the standard receiver application. Test each receiver with the standard receiver application. The receivers have to be connected to the PC using the USB3 port. The LAN connection of the receiver is not supported in the coherent mode. For details of installation of the receivers please refer to the WiNRADiO G65DDC User's Guide.

There are two topologically distinct ways in which the coherent receivers can be connected to the PC over the USB3 interface. The first way is the standard installation, where all coherent receivers are connected to the same PC, which allows for centralized processing of coherent signals.

The second way is the Extended Topology Configuration (ETC), where each receiver is connected to a separate dedicated PC. This allows for implementation of advanced parallel computing algorithms for phase-coherent systems. For more information on the Extended Topology Configuration (ETC) please refer to Chapter 5 of this document.

4 Extended installation of up to sixteen receivers

To install more than eight and up to sixteen receivers as a single coherent group, two WiNRADiO Coherence Clock & 1PPS Kits (**WR-CC1PPS-210e** as described in chapter 2.2) are needed. Two coherent clock generator units are interconnected and act as single coherent clock generator unit providing 16 outputs of the coherent sampling clock.

It is strongly recommended that you completely read chapter 3 before continuing to read this chapter. This chapter covers only the differences between the standard and extended installations. It is therefore necessary to perform the installation as described in chapter 3.

4.1 Connecting two Coherent clock generator units

As mentioned earlier, two Kits are needed to connect from 9 to 16 receivers as single coherent group of receivers. In such a configuration, one of the coherent clock generator units acts as master, other one acts as a slave.

A hook up diagram of two coherent clock generator units is shown in Picture 4-1. The master unit generates the sampling clock. The sampling clock from the two LO OUT ports is then distributed to both master CLK IN and slave CLK IN ports. **Use two identical SMA patch cables** for coherent clock distribution as described in Section 2.2.2 to interconnect both LO OUT outputs on the master unit to the CLK IN input on both master and slave unit.

The function of the **master** coherent clock generator unit is exactly the same as in a single unit configuration as described in 'chapter 3 Installation'. It generates the sampling clock and distributes it to eight receivers. It also generates the frequency reference if an external frequency reference is not used.

When using an external frequency reference, connect it to the master coherent clock generator unit only.

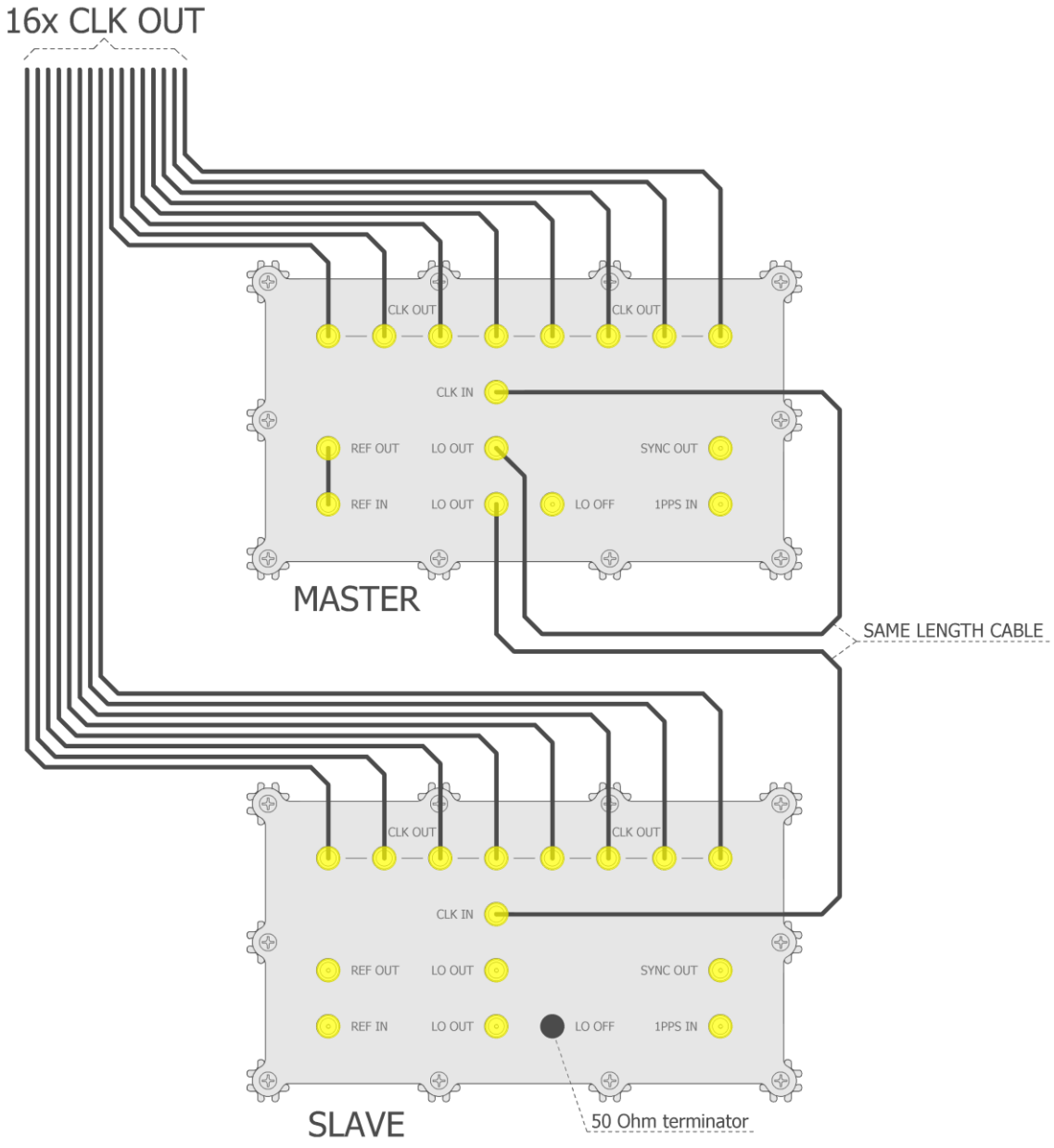
Similarly, if using the 1PPS signal, connect it to the 1PPS IN port on the master unit. The master distributes the signal from the 1PPS input through its SYNC OUT port to the receivers. Therefore, if using a 1PPS signal, connect the SYNC OUT to the SYNC IN port of the receiver which is the first in the synchronization chain as described in Section 3.4. If a 1PPS signal is unused, the 1PPS IN port and SYNC OUT ports can be left unconnected.

On the other hand, the function of the **slave** coherent clock generator unit is solely to distribute the sampling clock received on the CLK IN port of the slave unit to the receivers. The sampling clock is not generated on the slave unit. Therefore, it is necessary to interconnect the LO OUT port of the master to the CLK IN port of the slave unit as mentioned earlier and shown in Picture 4-1.

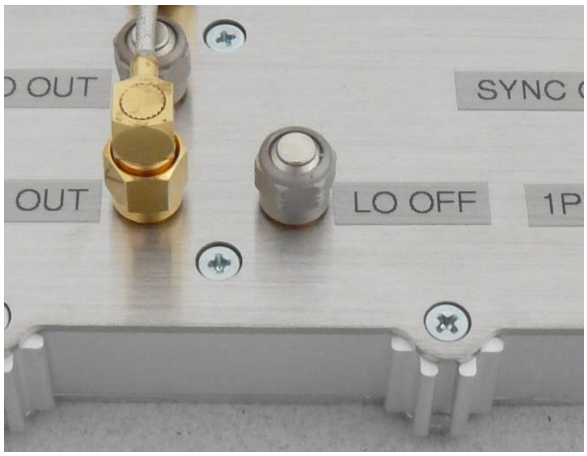
The sampling clock oscillator has to be turned off on the slave unit to prevent interference. This is done by installing the 50 ohm terminator onto the LO OFF port of the slave unit. The LO OFF port is used to disable the sampling clock oscillator and is described in Section 2.2.1.9 with the terminator is described in Section 2.2.4. The installed terminator is shown in picture 4-2.

No other ports on the slave unit are utilized in this extended installation. The ports REF IN, REF OUT, 1PPS IN, SYNC OUT as well as both LO OUT ports on a slave unit have to be left unconnected. Alternatively, 50 ohm terminators can be connected to these unused ports, however this is not mandatory.

When two coherent clock generator units are connected as show in Picture 4-1, all sampling clock outputs on both units are equivalent; therefore, any receiver within a coherent group can be connected to any of these ports on both units. However, unused CLK OUT ports have to be terminated using a 50 ohm SMA terminators for proper operation.



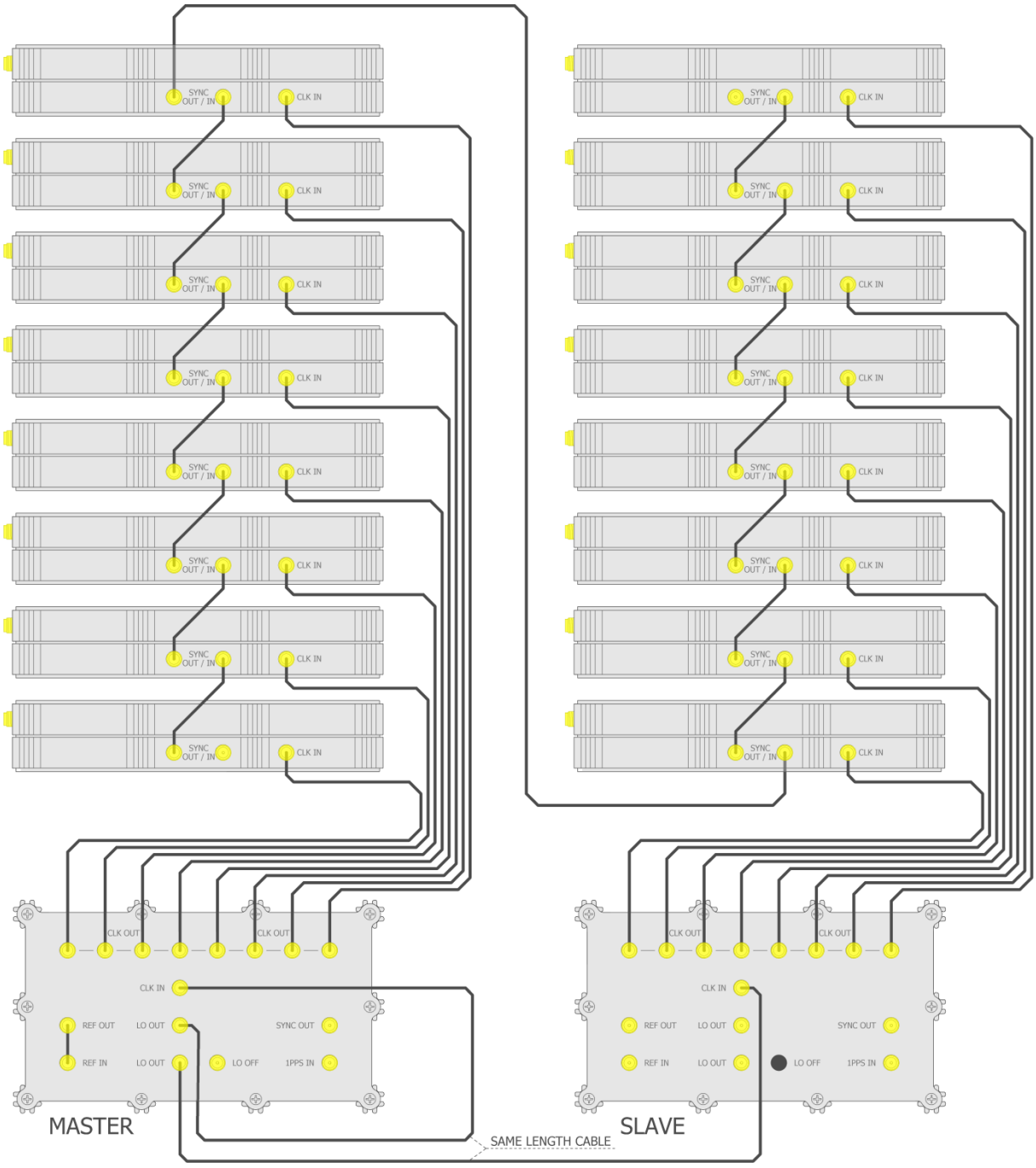
Picture 4-1: Interconnecting sampling clocks of two coherent clock generator units



Picture 4-2: The terminator for disabling the sampling clock oscillator is installed on the LO OFF port on the slave unit

4.2 Installation of receivers

For installation of up to sixteen receivers please refer to Picture 4-3 and Chapter 3 of this document. Please note that the sampling clock interconnects in picture 4-3 are drawn for clarity and there is no need to connect the sampling clock input of any particular receiver to any specific position on any sampling clock generator unit. Instead, all sampling clock outputs on both units are equivalent and can be connected to any receiver as convenient. Any unused CLK OUT ports on both master and slave unit have to be terminated using the 50 ohm SMA terminators for proper operation.



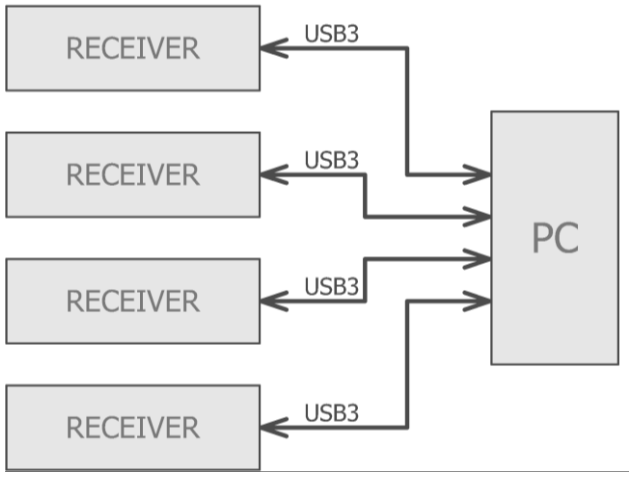
Picture 4-3: Sampling clock and digital sync signal interconnection of sixteen WR-G65DDCe receivers

5 Extended topology configuration (ETC)

There are two topologically distinct ways in which the coherent receivers can be connected to the PC over the USB3 interface. The first way is the standard installation, where all coherent receivers are connected to the same PC. The second way is the Extended Topology Configuration (ETC), where each receiver is connected to a separate dedicated PC. The differences between the two are explained below.

Please note, that the difference in both the standard and ETC configuration is only in the way the receivers are connected to the PC. All other aspects of coherent operation and connection described in the earlier chapters of this document remain the same for both configurations.

The **standard installation** of the WR-G65DDCe receivers in the coherent mode requires all receivers within the same coherent group to be connected to the same PC as shown in Picture 5-1. For most applications this standard installation is most beneficial, as all coherently received signals are available for centralized processing within one PC, thus reducing the overall complexity of implementation of the user application.



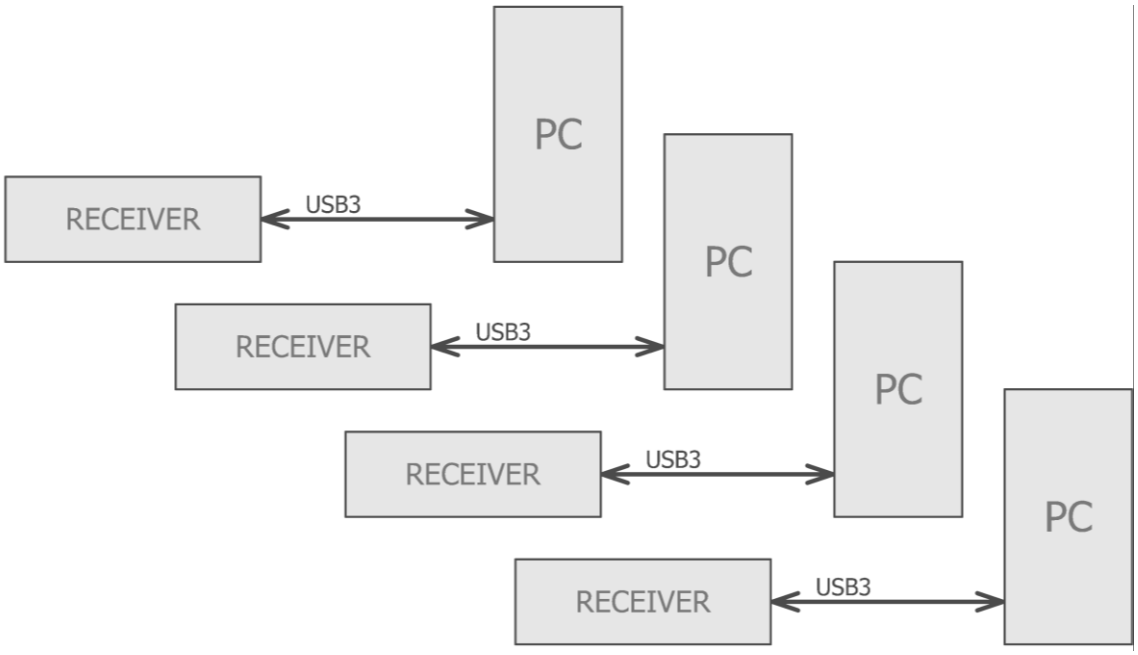
Picture 5-1: In standard installation, all receivers are connected to the same PC allowing for centralized coherent processing of received signals

The **Extended Topology Configuration (ETC)** for multichannel coherent operation of the WR-G65DDCe receivers allows the receivers to be connected to multiple PCs. Typically each WR-G65DDCe receiver is connected over the USB3 interface to a separate dedicated PC as shown in the Picture 5-2. Connection of multiple receivers to the same PC is allowed in the ETC configuration, however any receivers connected to the same PC act the same way as they would when connected to separate dedicated PCs. In other words, each receiver has to run its own instance of software. Also, it is not possible to mix the standard installation with the ETC installation. All necessary connections between the receivers and other supportive hardware are the same as described in previous chapters of this document.

The purpose of the ETC configuration is to allow for implementation of advanced parallel computing algorithms for phase-coherent systems as parallel multi-frequency and / or super-resolution estimation of direction of arrival, multi-frequency beam-forming and other applications requiring coherent reception of radio signals and their computation intensive processing. However, this introduces additional complexity of implementation of the user application because the coherently available received signals are distributed on multiple PCs. The user application is responsible for setting and synchronization of the receivers as well as for the transport of received coherent signals between the PCs, for further processing.

If each receiver in the same ETC multichannel system is installed into a separate computer, the user application can use TCP/IP or another form of communication between computers to achieve the proper setting and synchronization of the receivers as well as to transport the received signals between the computers for the processing of coherently received signals.

For more information on the ETC configuration please refer to the WR-G65DDC coherent mode SDK.



Picture 5-2: In Extended topology configuration, each receiver is connected to a separate dedicated PC

6 Technical specification

Output sampling frequency	210 MHz
Sampling clock output level	+2 dBm min. into 50 ohm
Number of sampling clock output ports	8
Reference frequency	10 MHz
REF IN input impedance	50 ohm
REF IN input level	+2 dBm min.
REF IN frequency tolerance	+/- 20 ppm
REF OUT output level	+4 dBm typ. into 50 ohm
Internal frequency reference stability	0.1 ppm
1PPS input impedance	50 ohm
1PPS input level L	0 – 0.8 V
1PPS input level H	2.1 V – 5 V
Power supply requirements	11 – 13 V DC @ 150 mA

7 Contacts

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