WiNRADiO®

WR-G35DDCi

Multichannel Coherent Application Guide

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1 Introduction

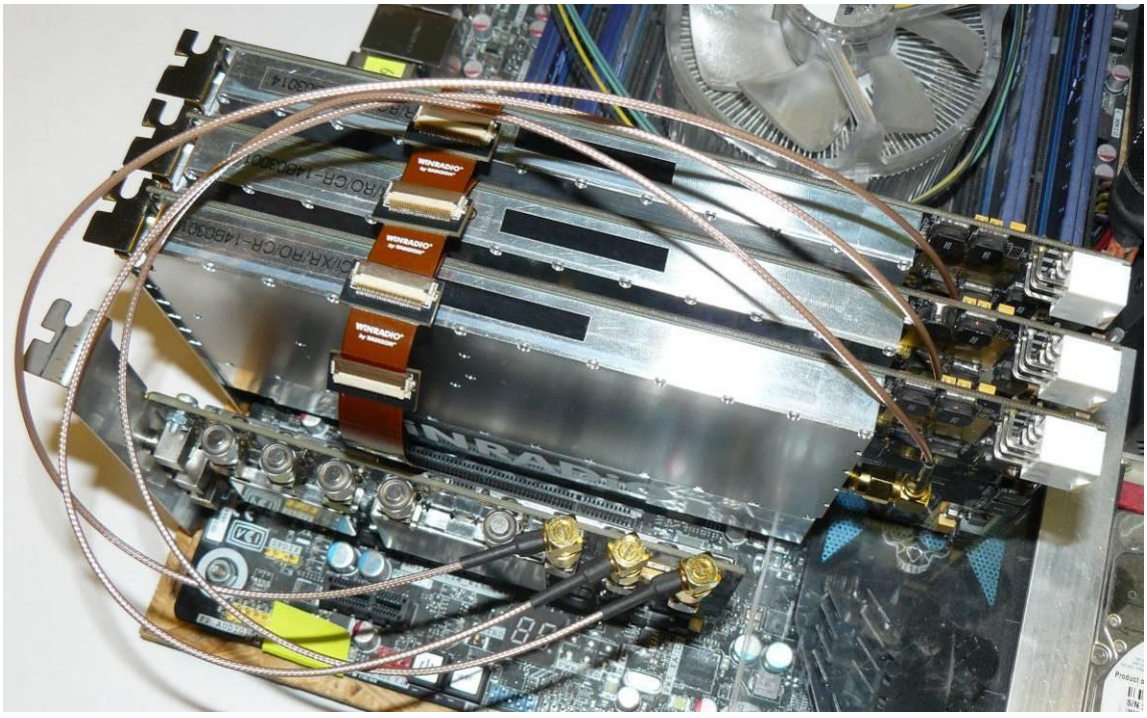
The WiNRADiO WR-G35DDCi receiver optionally provides multichannel coherent operation. A minimum of two and up to sixteen receivers can be coupled together for multichannel operation.

To couple up to eight receivers, the **WR-CC1PPS-100** 'WiNRADiO WR-G35DDCi Coherence Clock & 1PPS Kit' has to be used, which is described in section 2.2. To couple from nine to sixteen receivers, two Kits have to be used. For more than sixteen channels please contact WiNRADiO.

For coherent operation, all WR-G35DDCi receivers must be clocked at exactly the same frequency and phase. To achieve this requirement, it is necessary to distribute a sampling clock from a single low phase noise clock source. Therefore **the receivers have to be equipped with an ADC Clock Input Option (/CR)** for external sampling clock provision.

Similar to the sampling clock, all commands and operations of the receivers must be synchronized accordingly to the coherent sampling clock. For this reason the receivers have an external interconnection for digital synchronization, which is also provided on receivers with an ADC Clock Input Option (/CR)

An example of a coherent three channel system is shown in Picture 1-2.

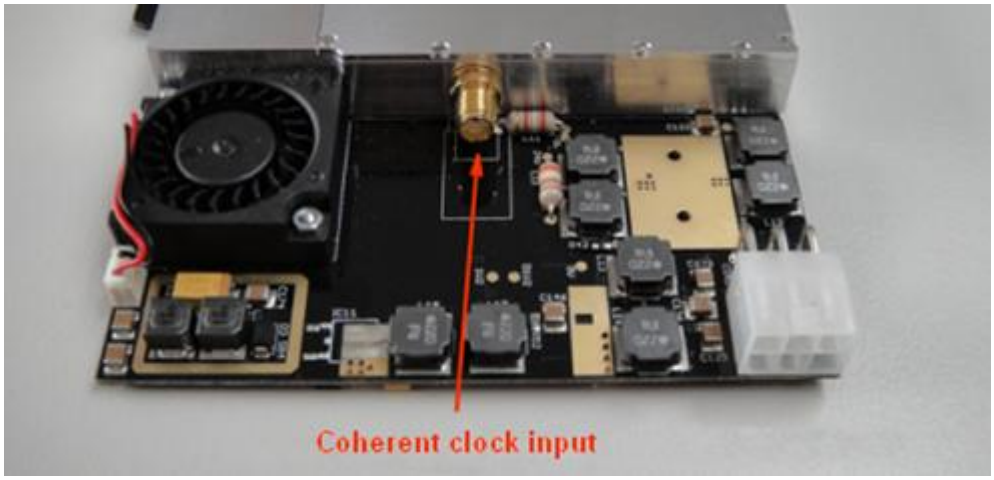


Picture 0-2: An example of three WR-G35DDCi receivers in coherent configuration, installed into a PC

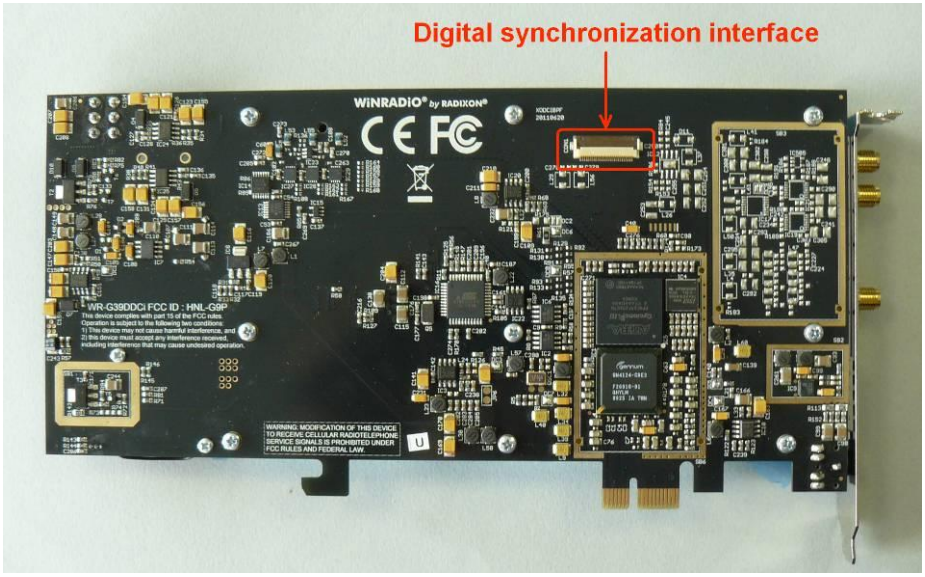
2 Parts description of the coherent system

2.1 WR-G35DDCi connectors

The connectors required for coherent operation of the WR-G35DDCi receivers are shown in Pictures 2-1 and 2-2 (present when the /CR option has been fitted):



Picture 2-1: Rear panel connectors of the WR-G35DDCi

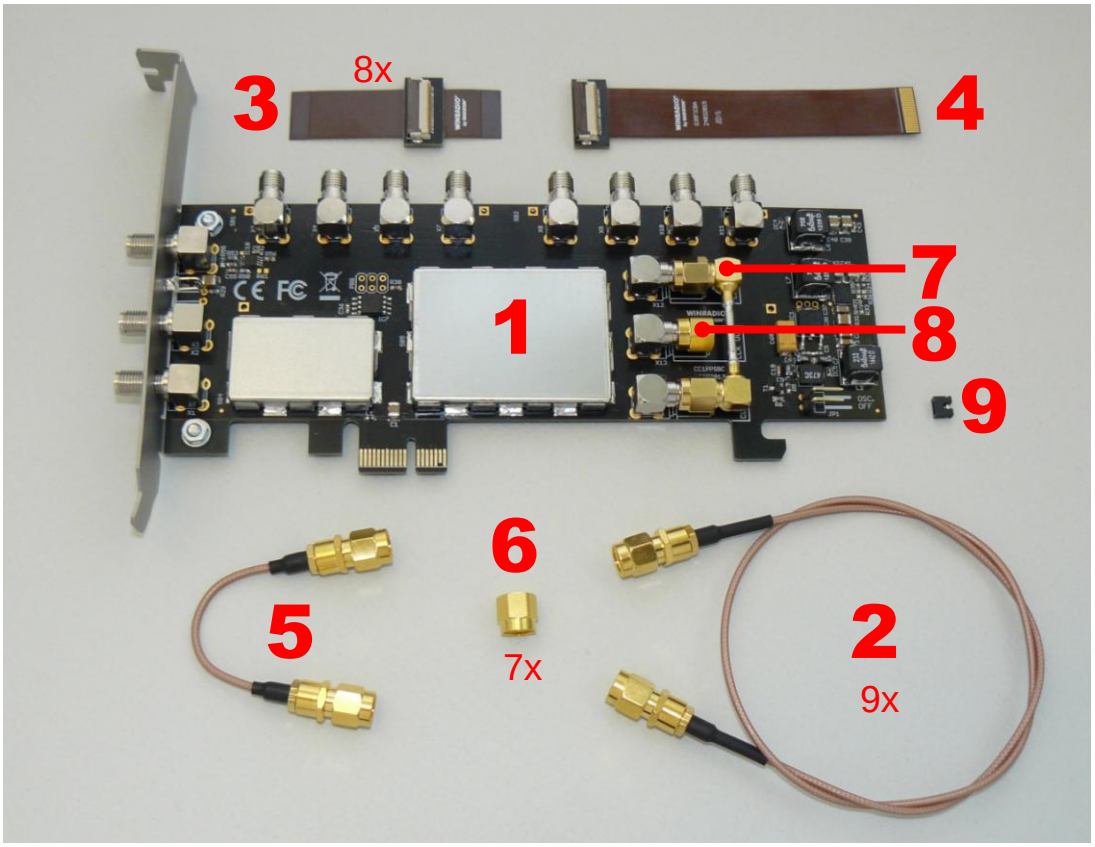


Picture 2-2: Digital synchronization connector of the WR-G35DDCi, viewed on the PCB side

2.2 The WiNRADiO Coherence Clock & 1PPS Kit (WR-CC1PPS-100)

The 'WiNRADiO Coherence Clock & 1PPS Kit' (hereafter referred to as the '**Kit**') provides production and distribution of a coherent 100 MHz clock for up to eight WR-G35DDCi receivers as well as digital synchronization of the receivers. It also features an internal frequency reference of 0.5 ppm stability, input for external frequency reference and digital input for a 1PPS pulse or external trigger pulse. The Kit consists of the following components (shown in Picture 2-3):

1. Coherent clock generator board with 1PPS input
2. SMA patch cables for coherent clock distribution (9 pcs)
3. Digital synchronization cables for each WR-G35DDCi receiver (8 pcs)
4. Digital synchronization cable for Coherent clock generator board
5. Frequency reference SMA interconnect cable
6. SMA terminators (7 pcs + 1 piece pre-installed on the board, see 8 below)
7. Sampling clock SMA coaxial jumper (factory pre-installed on the board)
8. Sampling clock SMA terminator (factory pre-installed on the board)
9. Standard circuit board jumper



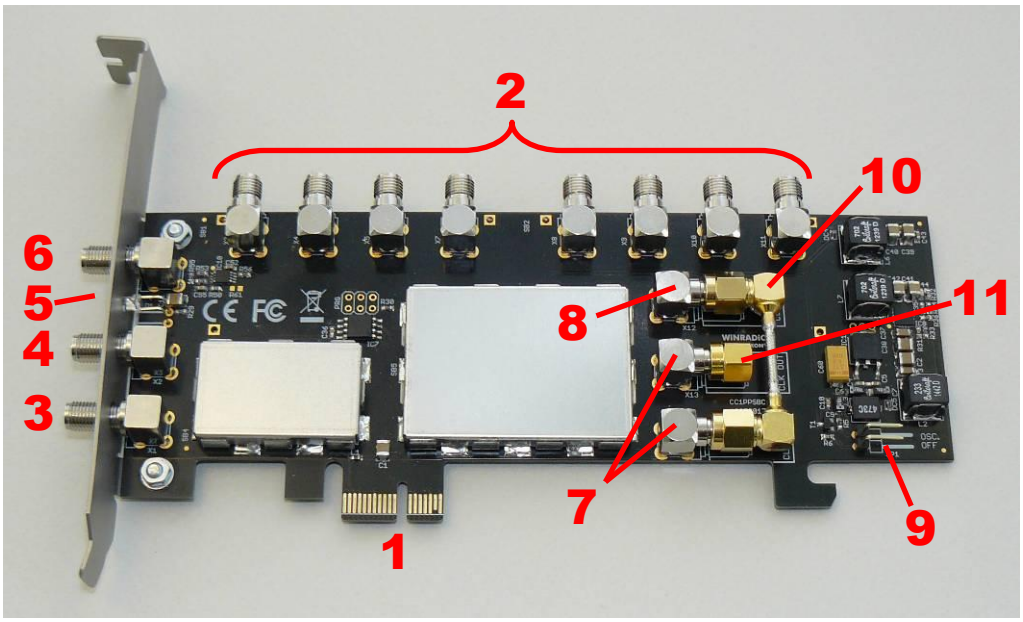
Picture 2-3: The WiNRADiO WR-G35DDCi Coherence Clock & 1PPS Kit

2.2.1 Coherent clock generator board with 1PPS input

The coherent clock generator board is shown in Picture 2-4. It is a PCIe card, which has to be installed into a PC together with WR-G35DDCi receivers. The board generates a 100 MHz sampling clock for up to eight WR-G35DDCi receivers. The sampling clock is locked to a frequency reference, which can be internal or external. It also distributes a 1PPS trigger signal from the 1PPS input to all connected WR-G35DDCi receivers via the digital synchronization interface.

No software driver is required for operation of the Coherent clock generator board.

For the technical specification of the board, please refer to chapter 5 of this document.



1 PCIe connector
2 SMA connectors for sampling clock output
3 Frequency reference output REF OUT
4 Frequency reference input REF IN
5 Locked indicator
6 1PPS trigger input
7 SMA connectors for local oscillator output
8 SMA connector for local oscillator input
9 Pin header for disabling the oscillator
10 Factory pre-installed SMA jumper
11 Factory pre-installed SMA terminator

Picture 2-4: Front view of Coherent clock generator board with 1 PPS input

2.2.2 PCIe connector

The PCIe connector provides power to the Coherent clock generator board. As there is no data communication running through the PCIe connector, no software driver is required for proper operation of the board. However, the board must be installed into a PCIe slot inside a PC.

2.2.3 SMA connectors for sampling clock output

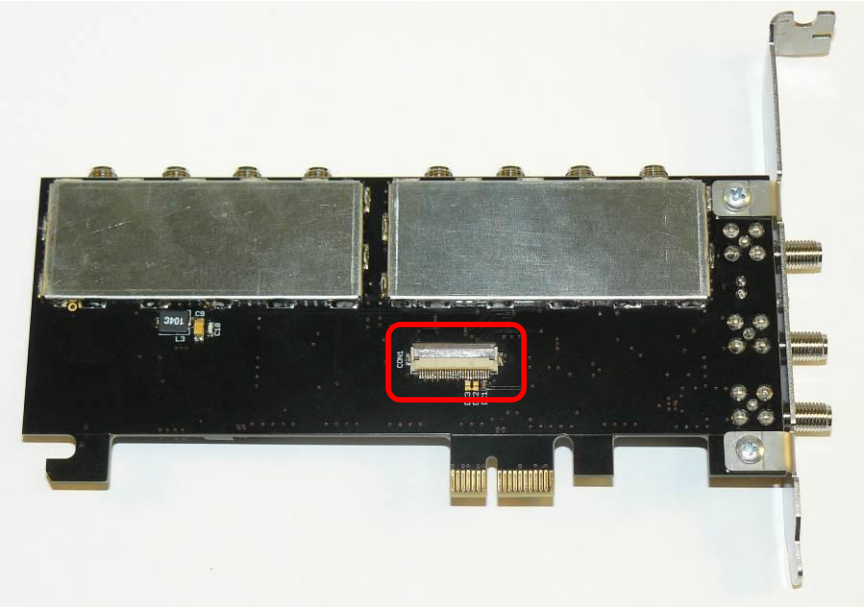
There are eight SMA connectors for the sampling clock output provided on the Coherent clock generator board. These are located on the top of the board and are facing upwards. Each WR-G35DDCi receiver within a coherent group must be connected to one of these ports using the SMA patch cables (for coherent clock distribution) supplied with the Kit and described in Section 2.2.9. All ports are equivalent; therefore any receiver within a coherent group can be connected to any of these ports. However, unused ports have to be terminated using the 50 OHM SMA terminators for proper operation.

For the technical specification of the sampling clock output signal, please refer to Chapter 5.

2.2.4 Digital synchronization interface

The digital synchronization interface is located on the rear side of the board. It provides a connection to the digital synchronization interconnection within a coherent group of receivers via the digital synchronization cable for the Coherent clock generator board (described in Section 2.2.10). It also distributes the 1PPS signal from the 1PPS input of the Coherent clock generator board to all WR-G35DDCi receivers within a coherent group. The digital synchronization cable for the coherent clock generator board attaches to this connector.

The synchronization protocol utilized on this interface is proprietary to WiNRADiO therefore no further specification is provided.



Picture 2-5: Rear view of Coherent clock generator board showing the location of the digital synchronization interface marked in red

2.2.5 Frequency reference output REF OUT

The frequency reference output is an SMA connector providing the 10 MHz (internal) frequency reference output signal. This output can be connected to the REF IN input port (Section 2.2.6) if the internal frequency reference operation of the board is required. Use the Frequency Reference SMA Interconnect cable (described in section 2.2.12 and provided with the Kit) to connect the REF OUT port to the REF IN port.

If unused, this port must be properly terminated using the 50 OHM terminator.

For the technical specification of the REF OUT, please refer to Chapter 5.

2.2.6 Frequency reference input REF IN

A signal provided to the frequency reference input REF IN serves as a frequency reference for the 100 MHz sampling clock generator. It is a 50 OHM terminated SMA connector. A 10 MHz reference signal must be provided on this input.

This input can be connected to the REF OUT output port (Section 2.2.5) if the internal frequency reference operation of the board is required. Use the Frequency Reference SMA Interconnect cable (described in section 2.2.12 and provided with the Kit) to connect the REF OUT port to REF IN port.

For the technical specification of the REF IN input, please refer to Chapter 5.

2.2.7 1PPS trigger input

The 1PPS trigger input is provided for applications which require external synchronization (using 1PPS signal from GPS or similar source) or require external triggering. It is a 50 OHM terminated SMA connector, which accepts 5V TTL logic levels.

The signal provided to this input is processed by a fast logic comparator and then distributed to all receivers within a coherent group of receivers over the Digital synchronization interface.

If unused, this port can be left unconnected.

For the technical specification of the input, please refer to Chapter 5.

2.2.8 Locked indicator

The 'Locked' indicator is lit whenever the 100 MHz sampling clock generator is locked to the frequency reference signal provided at the REF IN port. For more information about the REF IN port please refer to section 2.2.6.

2.2.9 SMA patch cables for coherent clock distribution

There are nine SMA patch cables supplied with the Kit. These are used to distribute the sampling clock from the Coherent clock generator board to all WR-G35DDCi receivers which are in coherent operation.

For interconnection, only use the original WiNRADiO SMA patch cables supplied with the Kit as these are specially matched to be coherent.

Picture 2-6: WiNRADiO coherent SMA patch cable

2.2.10 Digital synchronization cables for each WR-G35DDCi receiver

There are eight digital synchronization cables supplied with the Kit. These are used to synchronize all commands and operations of the WR-G35DDCi receivers within a coherent group. A single digital synchronization cable is needed for each WR-G35DDCi receiver. The cable attaches to the digital synchronization interface of the WR-G35DDCi receiver (see Picture 2-2).

For installation of the cable please refer to chapter 3 of this document.

Picture 2-7: Digital synchronization cable for the WR-G35DDCi receiver

2.2.11 Digital synchronization cable for the Coherent clock generator board

The function of the digital synchronization cable for the Coherent clock generator board is similar to the function of the digital synchronization cable for the WR-G35DDCi receivers described in the previous section. The difference is in its length and number of connectors (2 instead of 3) as it completes the digital synchronization chain of a group of coherent WR-G35DDCi receivers. It also distributes the 1PPS signal from the 1PPS input of the Coherent clock generator board to all WR-G35DDCi receivers within the coherent group. The cable attaches to an external interconnection interface of the Coherent clock generator board (Picture 2-5).

For installation of the cable please refer to chapter 3 of this document.

Picture 2-8: Digital synchronization cable for Coherent clock generator board

2.2.12 Frequency reference SMA interconnect cable

The frequency reference SMA interconnect cable is used to interconnect the internal reference output REF OUT of the Coherent clock generator board to the frequency reference input REF IN of the same board after it is installed into a PC. If an external frequency reference is used, this cable is not needed and should be kept safely, in case internal reference operation is required in the future.

For installation of the cable please refer to chapter 3 of this document.

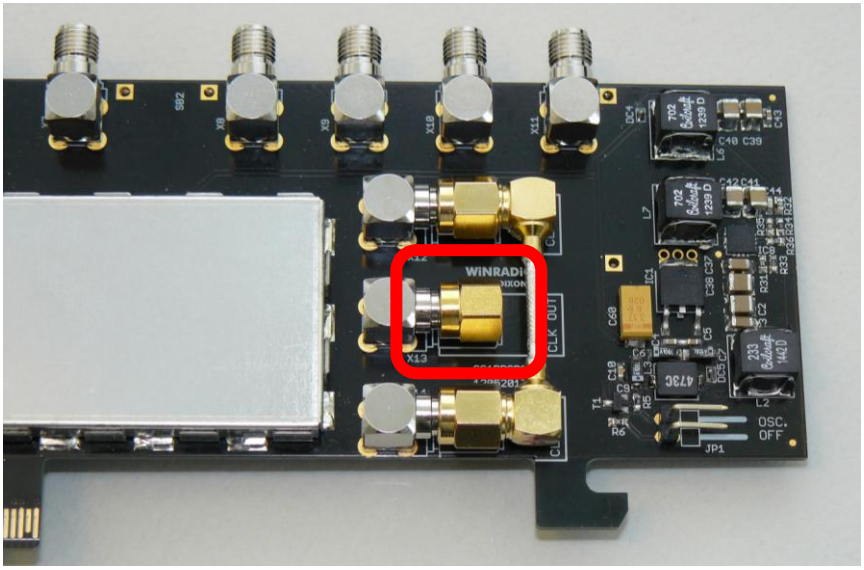
Picture 2-9: SMA interconnect cable for frequency reference

2.2.13 SMA terminators

The Kit comes with eight 50 OHM SMA terminators. These terminators must occupy all unused sampling clock outputs on the Coherent clock generator board. A minimum of two WR-G35DDCi receivers can be connected as a coherent pair, so six terminators are needed to terminate the sampling clock outputs. A seventh terminator is provided in case the external reference is used with the Coherent clock generator board. In such a case, the terminator must be installed on the REF OUT port of the Coherent clock generator board.

Picture 2-10: SMA terminators

The eighth terminator comes factory pre-installed on the Coherent clock generator board, terminating the secondary sampling clock oscillator output as shown in picture 2-11.



Picture 2-11: SMA terminator (marked in red) factory pre-installed on the secondary sampling clock oscillator output

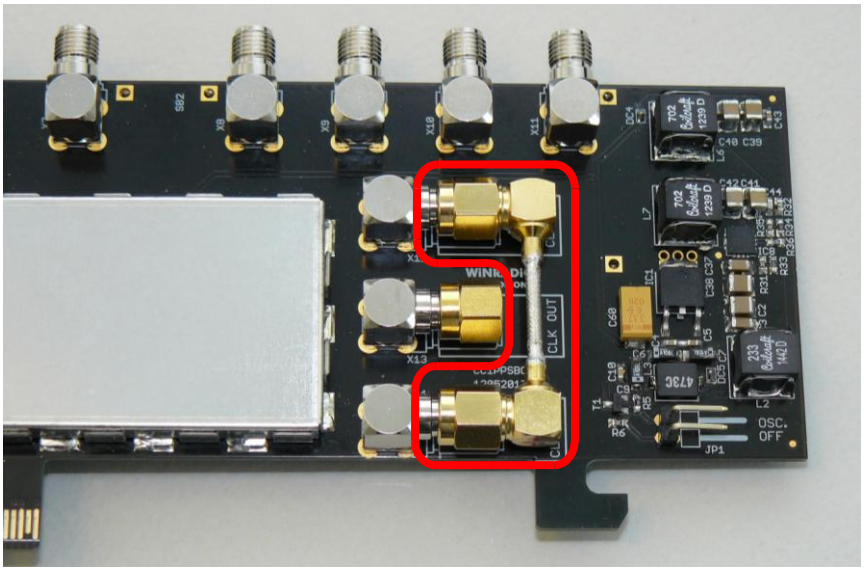
2.2.14 Sampling clock oscillator input and outputs

There are two sampling clock oscillator outputs and one input for the sampling clock oscillator on the coherent clock generator board. These are factory connected as shown in Picture 2-12 using SMA jumper cable as described in section 2.2.15 and one SMA 50 OHM terminator.

The factory connection need not to be altered for normal operation when using the coherent clock generator board to drive up to eight coherent receivers.

The purpose of these is to enable the use of **two coherent clock generator boards** to coherently drive up to sixteen receivers. For details on how to use two coherent clock generator boards to drive up to sixteen receivers please refer to chapter 4 of this document.

The factory connection consists of one 50 OHM terminator installed on one of the sampling clock outputs and an SMA jumper cable as described in section 2.2.15. This interconnects the sampling clock from the sampling clock oscillator output to the input of the sampling clock oscillator.



Picture 2-12: Factory pre-installed SMA jumper cable interconnecting (marked in red) the primary sampling clock oscillator output with the sampling clock oscillator input. Please note the mandatory terminator installed on the secondary sampling clock oscillator output.

2.2.15 SMA jumper cable

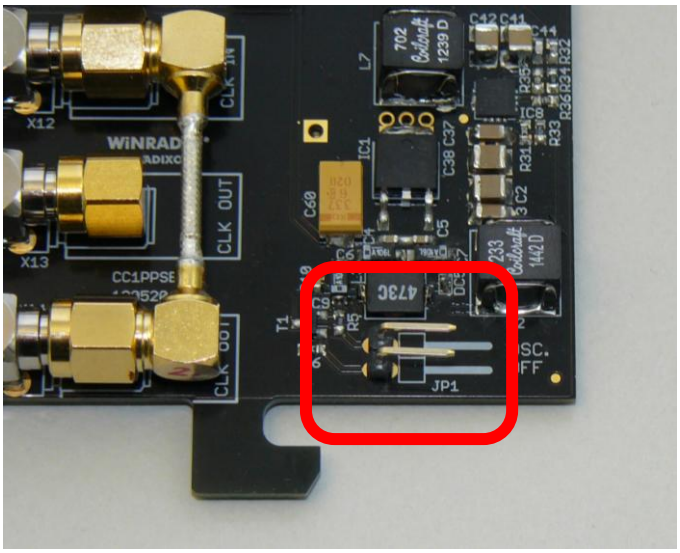
The Kit comes with an SMA jumper cable to connect the primary sampling clock oscillator output to the sampling clock oscillator output. This SMA jumper is factory pre-installed and is shown in picture 2-12. The jumper must be replaced with a proper patch cable when using two Coherent clock generator boards to distribute the sampling clock to up to sixteen

receivers. For details on how to use two coherent clock generator boards to drive up to sixteen receivers please refer to chapter 4 of this document.

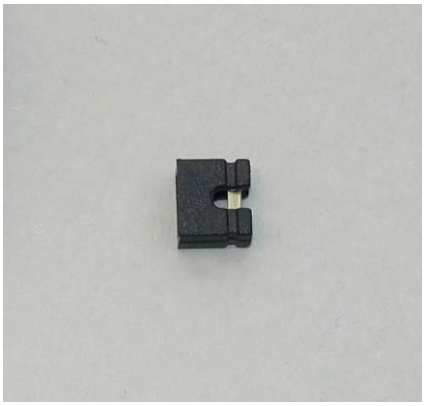
2.2.16 Pin header for disabling the sampling clock oscillator

The 'pin header' for disabling the sampling oscillator is shown in picture 2-13 and its corresponding jumper is shown in picture 2-14. No jumper is installed on the header for normal operation of a single coherent clock generator board.

The purpose of the pin header and its corresponding jumper is to provide the ability to turn off the local sampling clock oscillator on one of the coherent clock generator boards when two coherent clock generator boards are used to coherently drive up to sixteen receivers. For details on how to use two coherent clock generator boards to drive up to sixteen receivers please refer to chapter 4 of this document.



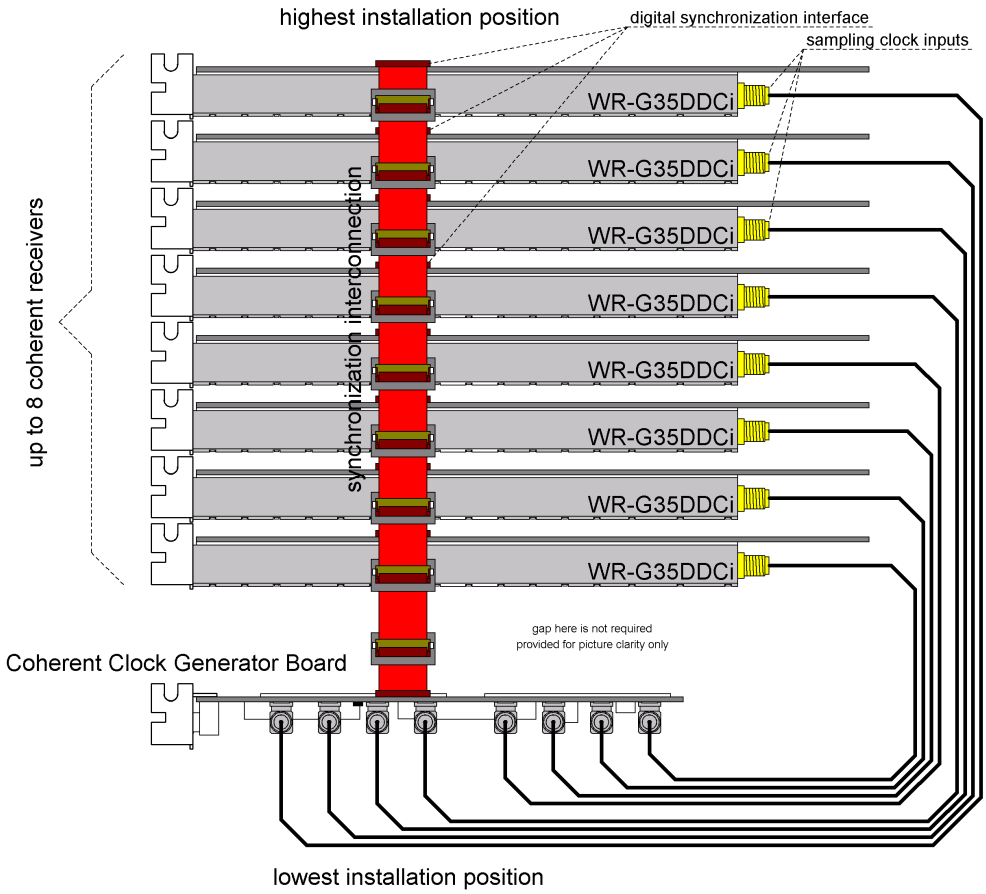
Picture 2-13: Pin header for disabling the sampling clock oscillator (marked in red)



Picture 2-14: Jumper for disabling the sampling clock oscillator

3 Standard installation of up to eight receivers

The basic setup of eight receivers is shown in Picture 3-1. The setup consists of eight WR-G35DDCi receivers installed into PCIe slots inside the PC. They are interconnected by a digital synchronization cable described in sections 2.2.10 and 2.2.11 and connected to the Coherent clock Generator Board by eight SMA patch cables as described in section 2.2.9.



Picture 3-1: Sampling clock and digital sync signal interconnection of eight WR-G35DDCi receivers. Picture is drawn as viewed from top of the receivers installed in a PC.

3.1 Preparing the receivers for installation into a PC

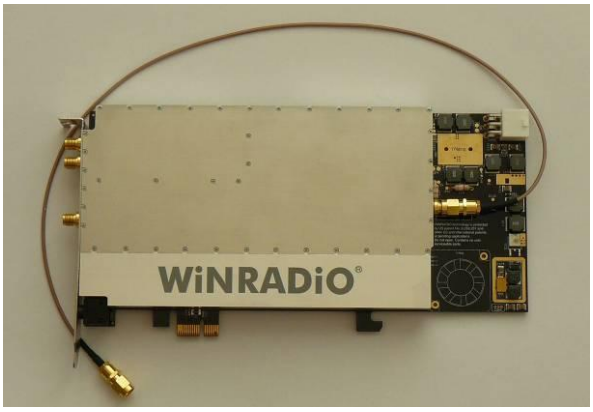
Prior to installation into a PC, please attach the SMA patch cable shown in Picture 2-6 to the coherent clock input of each receiver, leaving the other end of cable unconnected for now. The coherent clock input of the receiver is shown in Picture 2-1.

Please refer to Picture 3-2 for installation details.

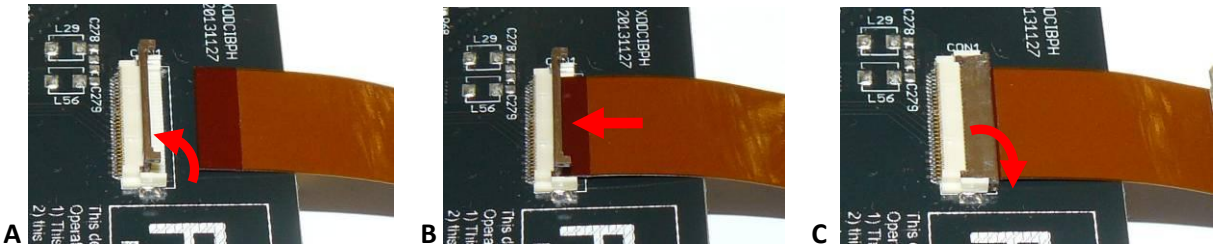
Also prior to installation into a PC, please attach the Digital synchronization cable to the digital synchronization port of each WR-G35DDCi receiver, also leaving the other end of cable unconnected for now. The digital synchronization interface connector is shown in

Picture 2-2. Please refer to Picture 3-4 for installation details. For FPC (Flat Printed-circuit Cable) connector installation instructions, please refer to Picture 3-3.

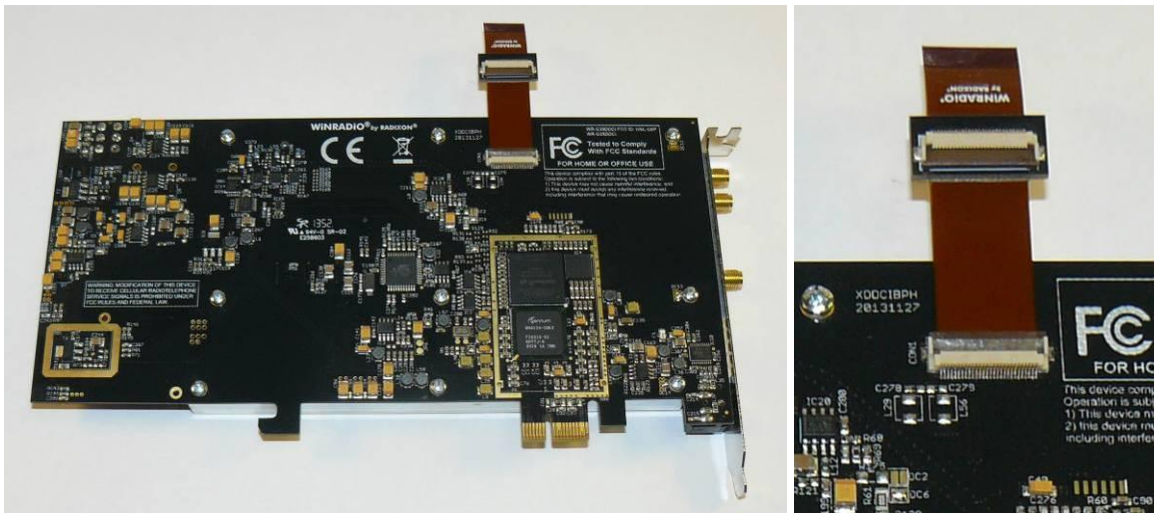
These two steps must be performed for each WR-G35DDCi receiver prior to installation into the PC because the coherent clock input and digital synchronization port of each receiver becomes inaccessible when multiple receivers are installed into a PC.



Picture 3-2: Sampling clock patch cable installed onto a receiver



Picture 3-3: Installing the FPC connector



Picture 3-4: Digital synchronization cable installed onto a receiver.

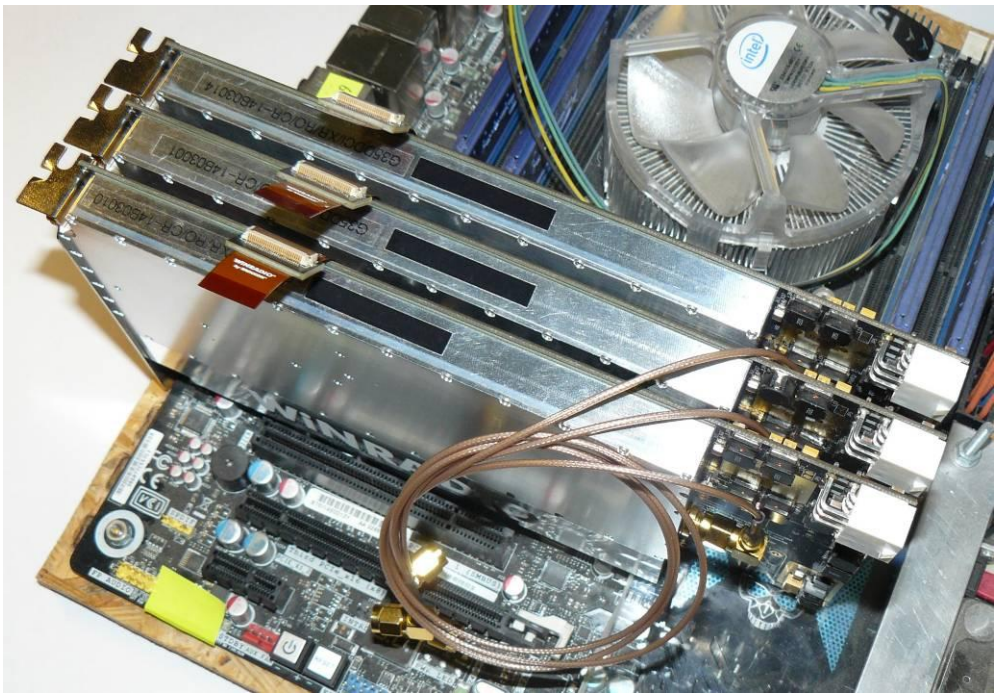
3.2 Installing the receivers into the PC

The PC has to be powered off when installing the receivers into PCIe slots.

The receivers have to be prepared for installation as discussed in section 3.1.

As shown in Picture 3-1, start with the physically highest receiver by installing it into a PCIe slot of the PC leaving both sampling clock cable and digital synchronization cable unconnected. Continue by installing the second (lower) receiver into the PC and again leaving both sampling clock cable and digital synchronization cable unconnected. Continue to the final receiver, always leaving both sampling clock cable and digital synchronization cables unconnected.

For details of receiver installation into a PC PCIe slot, please refer to the WR-G35DDCi user guide.

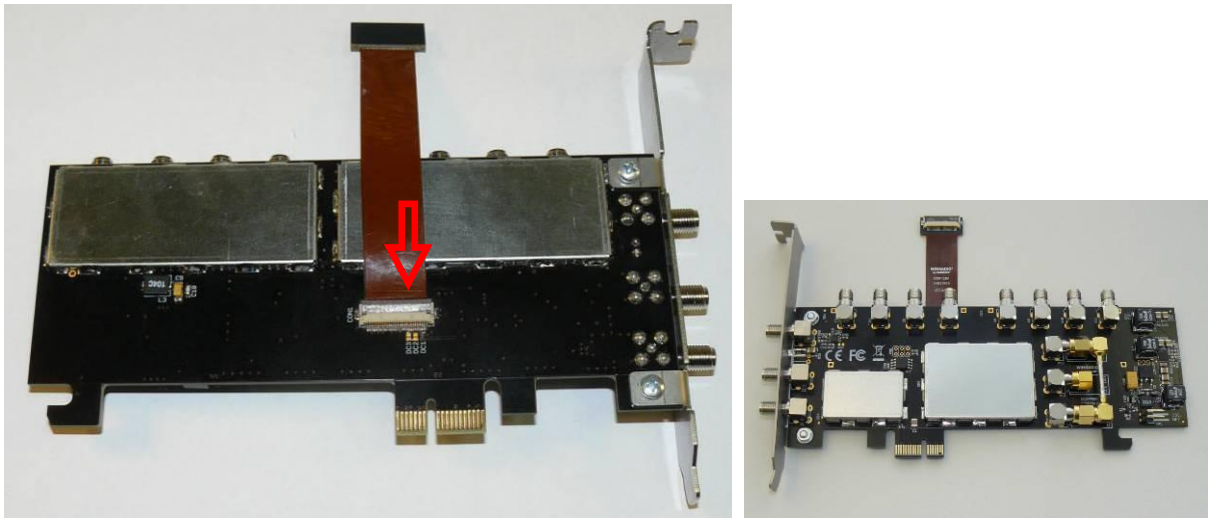


Picture 3-5: Receivers installed into the PC

3.3 Installing the digital synchronization cable onto the coherent clock generator board

Prior to installation into a PC, please attach the Digital synchronization cables for the Coherent clock generator board to the digital synchronization port of the Coherent clock generator board, leaving the other end of cable unconnected for now. The digital synchronization interface connector of the Coherent clock generator board is shown in Picture 2-5. Please refer to Picture 3-6 for installation details.

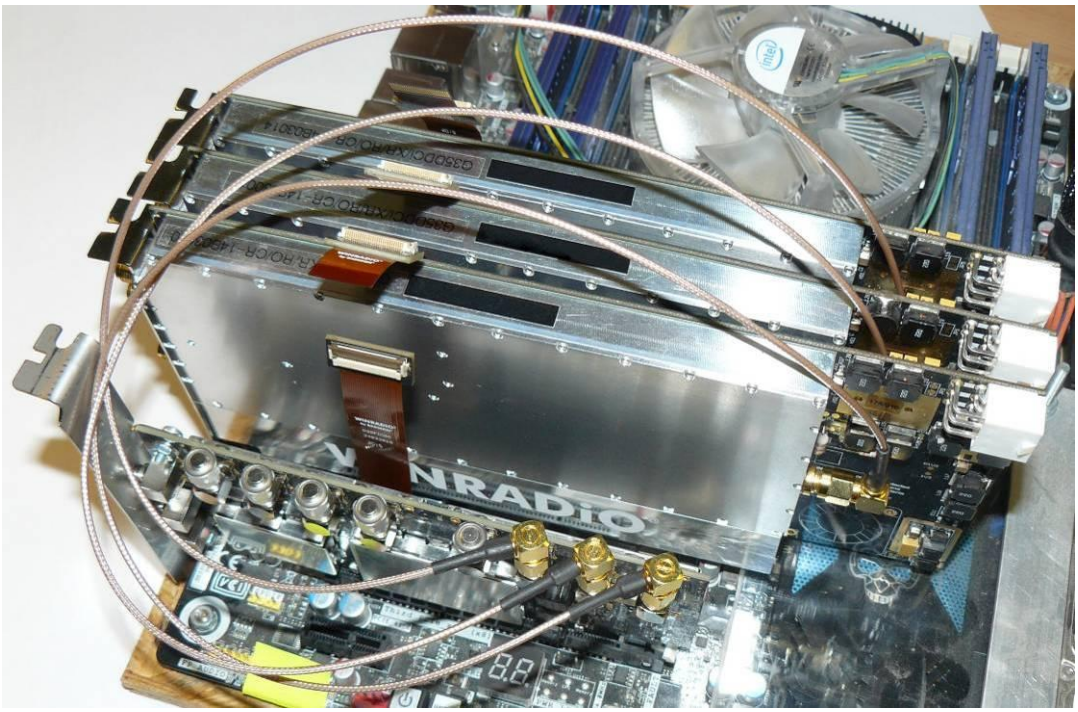
For FPC connector installation instructions, please refer to Picture 3-3.



Picture 3-6: Digital synchronization cable installed into the Coherent clock generator board

3.4 Connecting the coherent ADC sampling clock

Prior to installation of the Coherent clock generator board into the PC, connect the SMA patch cables of each receiver which has been installed into the PC (described in section 3.1) to the Coherent clock generator board as shown in Picture 3-7. Unused sampling clock out ports on the Coherent clock generator board have to be terminated using the 50 OHM SMA terminators for proper operation.



Picture 3-7: Installing the SMA patch cables for the coherent clock distribution into the coherent clock generator board

3.5 Installing the coherent clock generator board into the PC

The PC has to be powered off when installing the coherent clock generator board into PCIe slot.

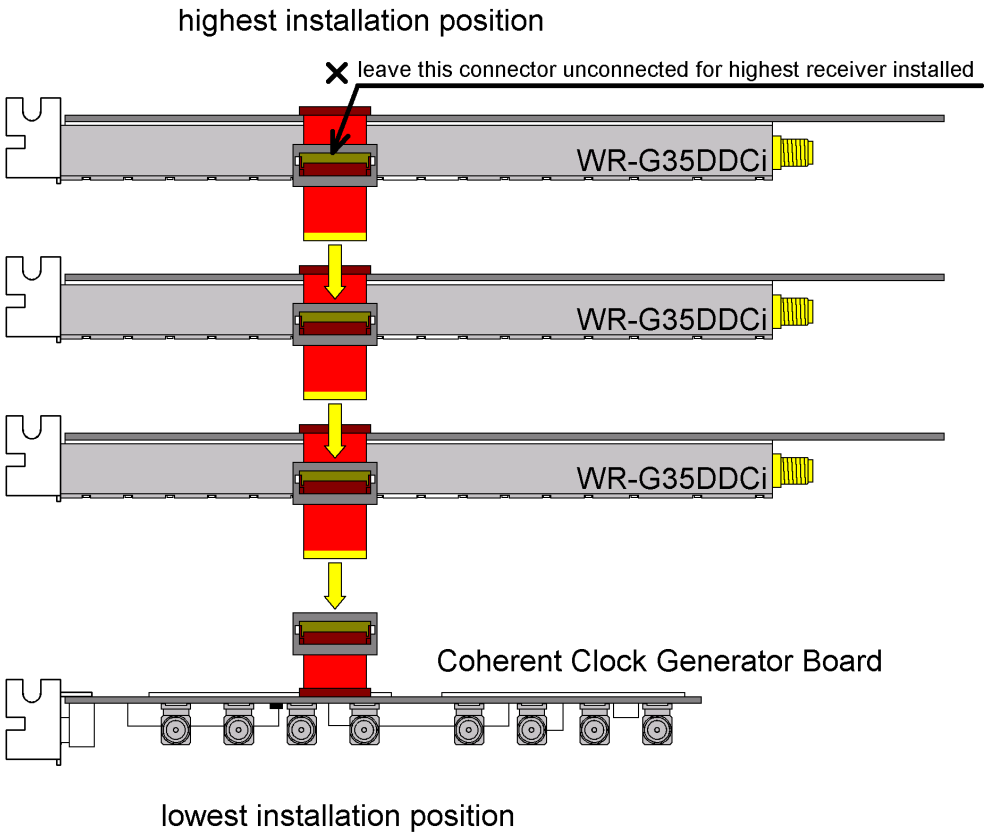
The coherent clock generator board has to be prepared for installation as described in the previous sections.

As shown in Picture 3-1, the coherent clock generator board has to be installed into the physically lowest position (by installing it into a PCIe slot of the PC leaving the digital synchronization cable unconnected).

3.6 Connecting the digital synchronization interconnection

Start by connecting the digital synchronization cable of the physically lowest receiver to the connector on the digital synchronization cable of the coherent clock generator board as shown in Picture 3-8. Continue by connecting the digital synchronization cable of the second lowest receiver to the connector of the digital synchronization cable. Continue by adding connections towards the highest installation position. Please leave the connector on the last (highest) receiver 'digital synchronization cable' unconnected.

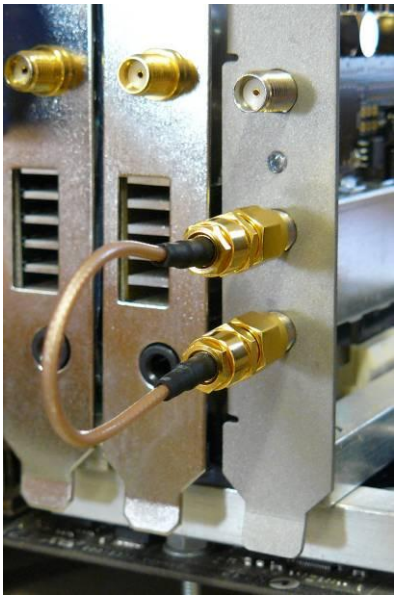
For FPC connector installation instructions please refer to Picture 3-3.



Picture 3-8: Connecting the digital synchronization interconnection

3.7 Choosing the frequency reference

When using the internal frequency reference, please connect the internal reference output REF OUT of the Coherent clock generator board to the frequency reference input REF IN of the board after it is installed into a PC as shown in Picture 3-9. Please use the Frequency reference SMA interconnect cable as described in section 2.2.12.



Picture 3-9: Installing the frequency reference SMA interconnect cable for internal frequency operation

When use of an external frequency reference is required, please connect the frequency reference signal to the REF IN port of the Coherent clock generator board as described in section 2.2.6. Please note that the REF OUT port has to be properly terminated using the 50 OHM terminator when unused.

3.8 Power up and driver installation

Turn the host PC on. The host PC will recognize each WR-G35DDCi unit as new hardware connected to it. For installation of the driver and software, please refer to the WR-G35DDCi software installation guide.

4 Extended installation of up to sixteen receivers

To install more than eight and up to sixteen receivers as a single coherent group, two WiNRADiO Coherence Clock & 1PPS Kits (as described in chapter 2.2) are needed. Two coherent clock generator boards are interconnected and act as single coherent clock generator board providing 16 outputs of the coherent sampling clock.

It is strongly recommended that you completely read chapter 3 before continuing to read this chapter. This chapter covers only the differences between the standard and extended installations. It is therefore necessary to perform the installation as described in chapter 3.

4.1 Connecting two Coherent clock generator boards

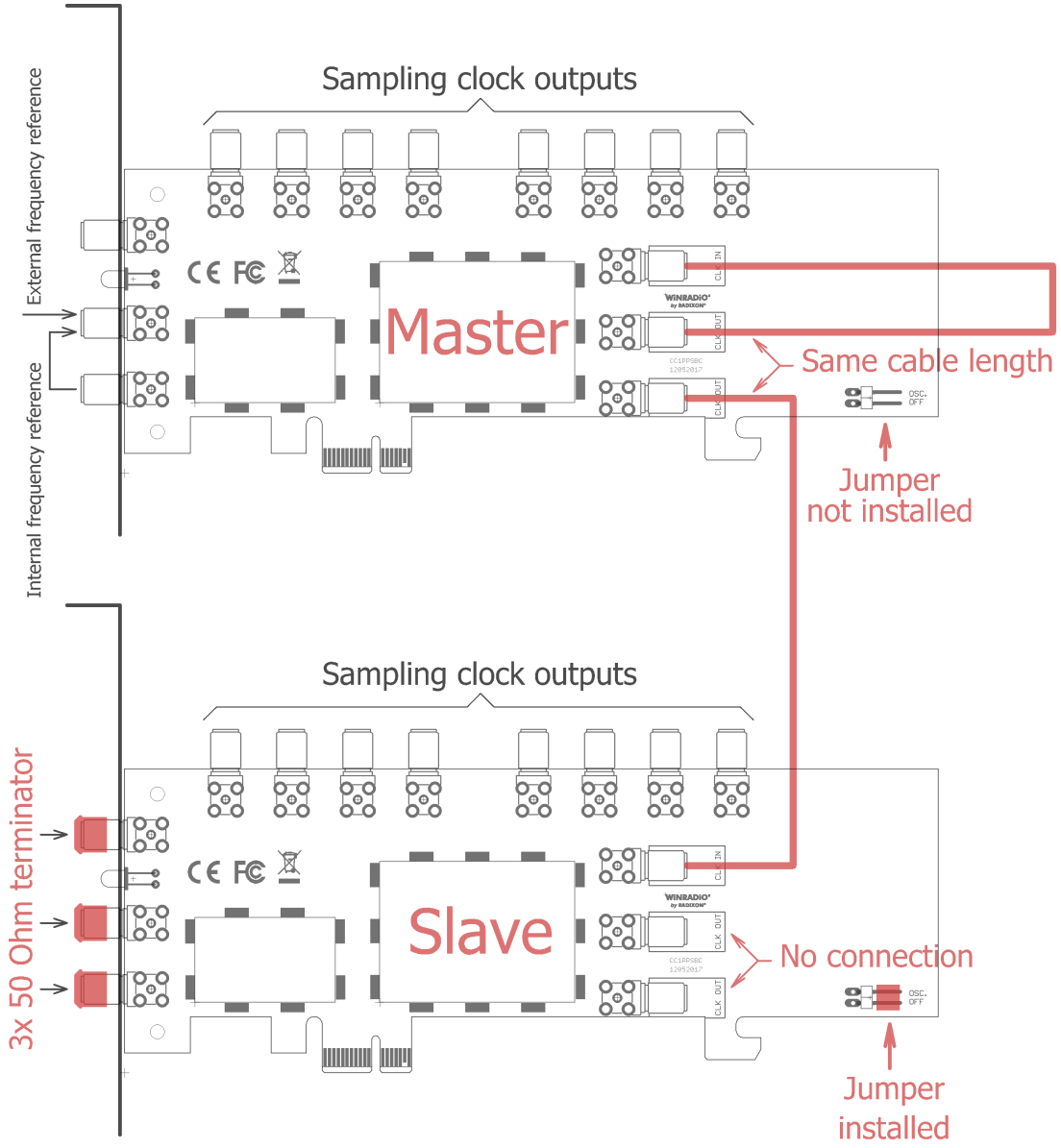
As mentioned earlier, two Kits are needed to connect from 9 to 16 receivers as single coherent group of receivers. In such a configuration, one of the coherent clock generator boards acts as master, other one acts as a slave.

The function of the master coherent clock generator board is exactly the same as in a single board configuration as described in 'chapter 3 Installation'. It generates the sampling clock and distributes it to eight receivers. It also distributes a signal from the 1PPS input and generates the frequency reference if an external frequency reference is not used. When using an external frequency reference, connect it to the master coherent clock generator board only.

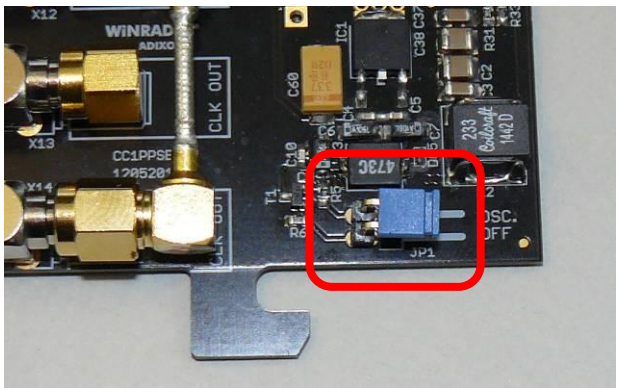
On the other hand, the function of the slave coherent clock generator board is solely to distribute the sampling clock to the receivers and the sampling clock is not generated on the slave board. The sampling clock is generated on the master and then fed to the slave board, which then distributes it to the other eight receivers. **The sampling clock oscillator has to be turned off on the slave board to prevent interference**. This is done by installing the jumper onto the pin header used for disabling the sampling clock oscillator. Both the pin header for disabling the sampling clock oscillator and the jumper are described in section 2.2.16 and shown in pictures 2-13 and 2-14. The installed jumper is shown in picture 4-2.

A hook up diagram of two coherent clock generator boards is shown in Picture 4-1. Use SMA patch cables for coherent clock distribution as described in section 2.2.9 to interconnect both boards. Please note that the same cable as used to interconnect master and slave boards needs to be used to interconnect the sampling clock output to the sampling clock input on a master board. Also 50 OHM terminators are needed on the slave board frequency reference output, frequency reference input and 1PPS input. The sampling clock oscillator outputs on a slave board can be left unconnected.

When two coherent clock generator boards are connected as show in Picture 4-1 all sampling clock outputs on both boards are equivalent; therefore any receiver within a coherent group can be connected to any of these ports on both boards. However, unused ports have to be terminated using the 50 OHM SMA terminators for proper operation.



Picture 4-1: Interconnecting sampling clocks of two coherent clock generator boards



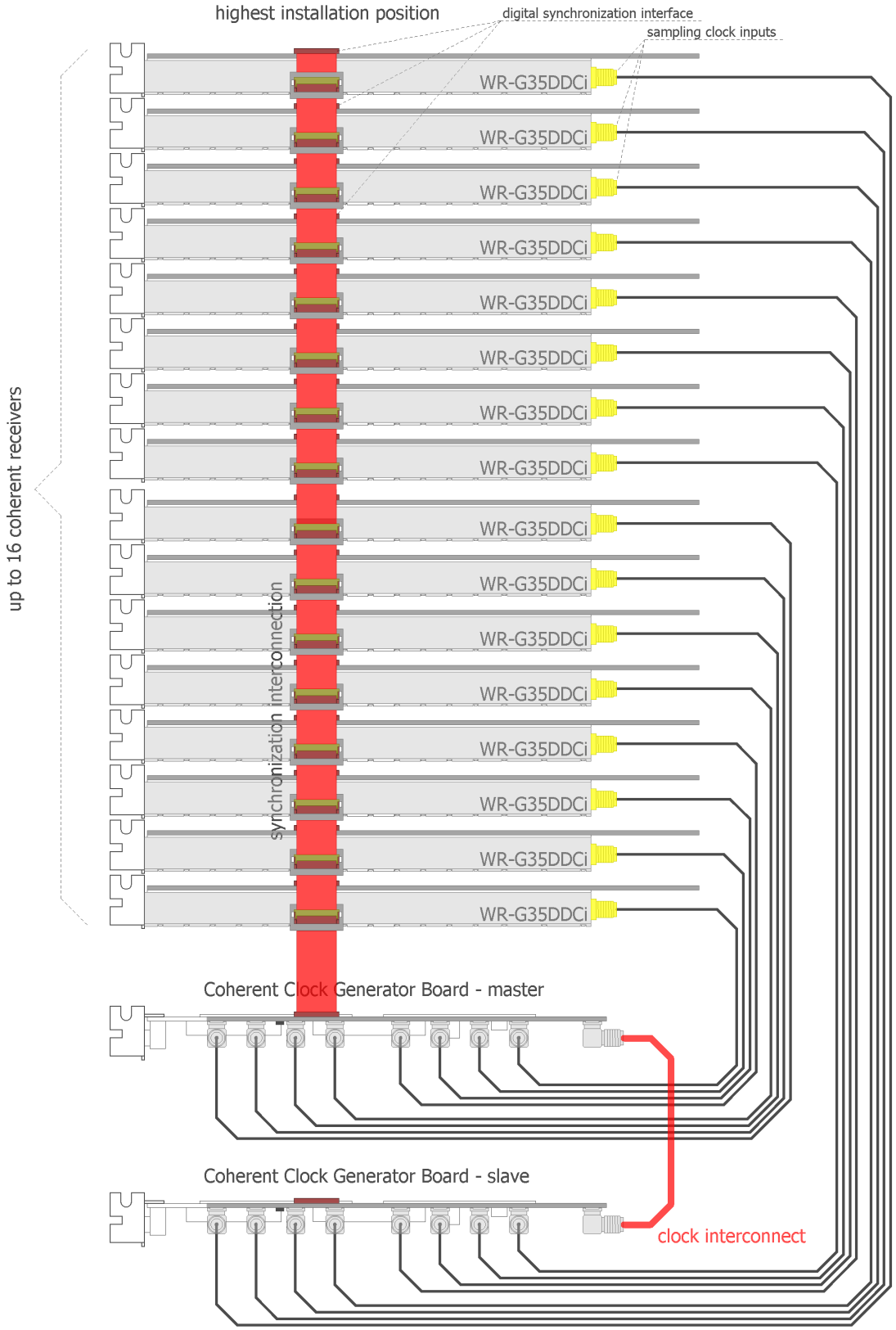
Picture 4-2: The jumper for disabling the sampling clock oscillator is installed on the slave board (marked in red). A blue jumper is used for picture clarity.

4.2 Installation of receivers

For installation of up to sixteen receivers please refer to Picture 4-3 and Chapter 3 of this document.

Please note that the slave coherent clock generator board does not connect through a digital synchronization interface; it only distributes the sampling clock. For digital synchronization interconnection as well as frequency reference input and output and 1PPS input, the master coherent clock generator board must be used.

Also please note that the sampling clock interconnects in picture 4-3 are drawn for clarity and there is no need to connect the sampling clock input of any particular receiver to any specific position on any sampling clock generator board. Instead, all sampling clock outputs on both boards are equivalent and it is recommended that receivers in the highest installation positions are first connected to the closest available sampling clock outputs on the master board. Unused ports have to be terminated using the 50 OHM SMA terminators for proper operation.



Picture 4-3: Sampling clock and digital sync signal interconnection of sixteen WR-G35DDCi receivers. Picture is drawn as viewed from top of the receivers installed in a PC. Clock interconnect (marked in red) is described in Section 4.1.

5 Technical specification

Output sampling frequency	100 MHz
Sampling clock output level	+2 dBm min. into 50 OHM
Number of sampling clock output ports	8
Reference frequency	10 MHz
REF IN input impedance	50 OHM
REF IN input level	+2 dBm min.
REF IN frequency tolerance	+/- 20 ppm
REF OUT output level	+4 dBm typ. into 50 OHM
Internal frequency reference stability	0.5 ppm
1PPS input impedance	50 OHM
1PPS input level L	0 – 0.8 V
1PPS input level H	2.1 V – 5 V

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