WiNRADiO®

WR-ETC-100

(for the G35DDCi)

Multichannel Coherent Application Guide for the Extended Topology Configuration option (ETC)

Version 1.0

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Introduction

The WiNRADiO WR-G35DDCi receiver optionally provides multichannel coherent operation. A minimum of two and up to sixteen receivers can be coupled together for multichannel operation.

This document does not describe the standard installation of WR-G35DDCi receivers for multichannel coherent operation. The standard installation of the WR-G35DDCi receivers in coherent mode requires all WR-G35DDCi receivers to be installed inside the same PC and all connections between receivers and other supportive hardware are realized internally, within the same PC. For standard installation please refer to WR-G35DDCi Multichannel Coherent Application Guide.

This document describes non-standard, **Extended Topology Configuration (ETC)** for multichannel coherent operation of the WR-G35DDCi receivers, which allows the receivers to be installed in multiple PCs. Typically, each WR-G35DDCi receiver is installed in a separate dedicated PC. Installation of multiple receivers inside the same PC is allowed in the ETC configuration, however any receivers installed inside the same PC act the same way as they would, when installed in separate dedicated PCs. In other words, each receiver has to run its own instance of software. Also, it is not possible to mix the standard installation with the ETC installation. All necessary connections between the receivers and other supportive hardware are realized externally, outside of the PCs.

To couple up to eight receivers, the **WR-CC1PPS-100** 'WiNRADiO WR-G35DDCi Coherence Clock & 1PPS Kit' (the Clock Kit) has to be used, which is described in Section 2.2. To couple from nine to sixteen receivers, two Clock Kits have to be used. For more than sixteen channels please contact WiNRADiO.

Moreover, in Extended Topology Configuration (ETC), each WR-G35DDCi receiver has to be equipped with the **WR-ETC-100** 'WiNRADiO Extended topology Configuration kit' (ETC kit). Therefore, for ETC configuration, the number of ETC kits needed is equal to number of WR-G35DDCi receivers in the coherent multichannel group. The ETC kit is described in Section 2.3. The purpose of the ETC kit is to allow for external distribution of the sampling clock and digital synchronization signals, outside of the PC.

For coherent operation, all WR-G35DDCi receivers must be clocked at exactly the same frequency and phase. To achieve this requirement, it is necessary to distribute a sampling clock from a single low phase noise clock source (from the Clock Kit). Therefore, **the receivers have to be equipped with an ADC Clock Input Option (/CR)** for external sampling clock provision.

Similar to the sampling clock, all commands and operations of the receivers must be synchronized accordingly to the coherent sampling clock. For this reason, the receivers have an external interconnection for digital synchronization, which is also provided on receivers with an ADC Clock Input Option (/CR).

An example of a one receiver, forming part of a multichannel coherent system in ETC configuration is shown in Picture 1-2.

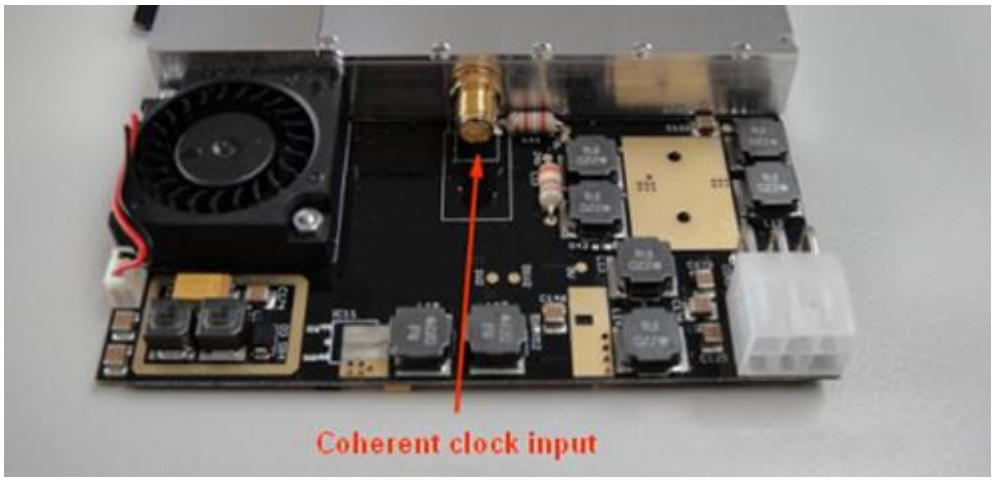
Picture 1-2: An example of a one WR-G35DDCi receiver, forming part of a multichannel coherent system in ETC configuration with the ETC kit, installed into a PC (PC chassis and other PC connections omitted for clarity). The WR-CC1PPS-100 kit is also required for coherent operation, but is not shown in this picture.

The coaxial cables (shown in the picture) which are connected to the ETC kit carry the sampling clock from the WR-CC1PPS-100 kit as well as the digital synchronization signals needed to coherently synchronize all of the receivers together. The synchronization signals are connected in a daisy chain manner; thus, two coaxial cables are needed to connect this particular receiver to its two neighbouring receivers.

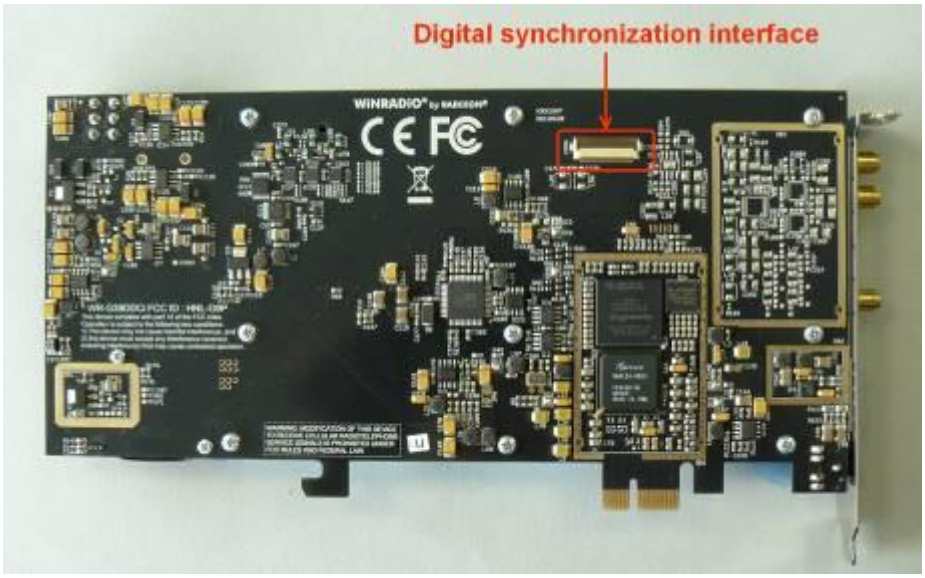
2. Parts description of the coherent system

2.1 WR-G35DDCi connectors

The connectors required for coherent operation of the WR-G35DDCi receivers are shown in Pictures 2-1 and 2-2 (present when the /CR option has been fitted):



Picture 2-1: Rear panel connectors of the WR-G35DDCi

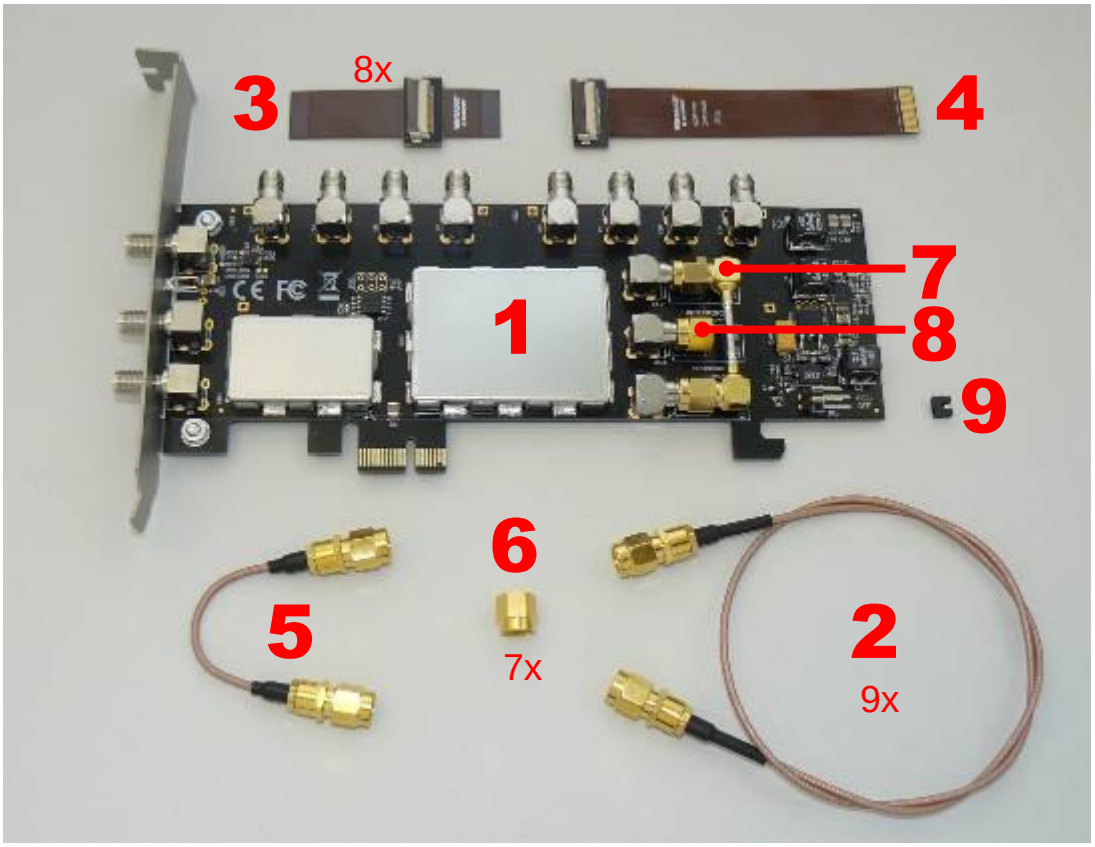


Picture 2-2: Digital synchronization connector of the WR-G35DDCi, viewed on the PCB side

2.2 The WiNRADiO Coherence Clock & 1PPS Kit (WR-CC1PPS-100)

The 'WiNRADiO Coherence Clock & 1PPS Kit' (hereafter referred to as the **'Clock Kit**') provides production and distribution of a coherent 100 MHz clock for up to eight WR-G35DDCi receivers as well as digital synchronization of the receivers. It also features an internal frequency reference of 0.5 ppm stability, input for external frequency reference and digital input for a 1PPS pulse or external trigger pulse. The Clock Kit consists of the following components (shown in Picture 2-3):

1. Coherent clock generator board with 1PPS input
2. SMA patch cables for Coherent clock distribution (9 pcs)
3. Digital synchronization cables for each WR-G35DDCi receiver (8 pcs) – unused in ETC configuration
4. Digital synchronization cable for Coherent clock generator board – unused in ETC configuration
5. Frequency reference SMA interconnect cable
6. SMA terminators (7 pcs + 1 piece pre-installed on the board, see 8 below)
7. Sampling clock SMA coaxial jumper (factory pre-installed on the board)
8. Sampling clock SMA terminator (factory pre-installed on the board)
9. Standard circuit board jumper



Picture 2-3: The WiNRADiO WR-G35DDCi Coherence Clock & 1PPS Kit (the Clock Kit)

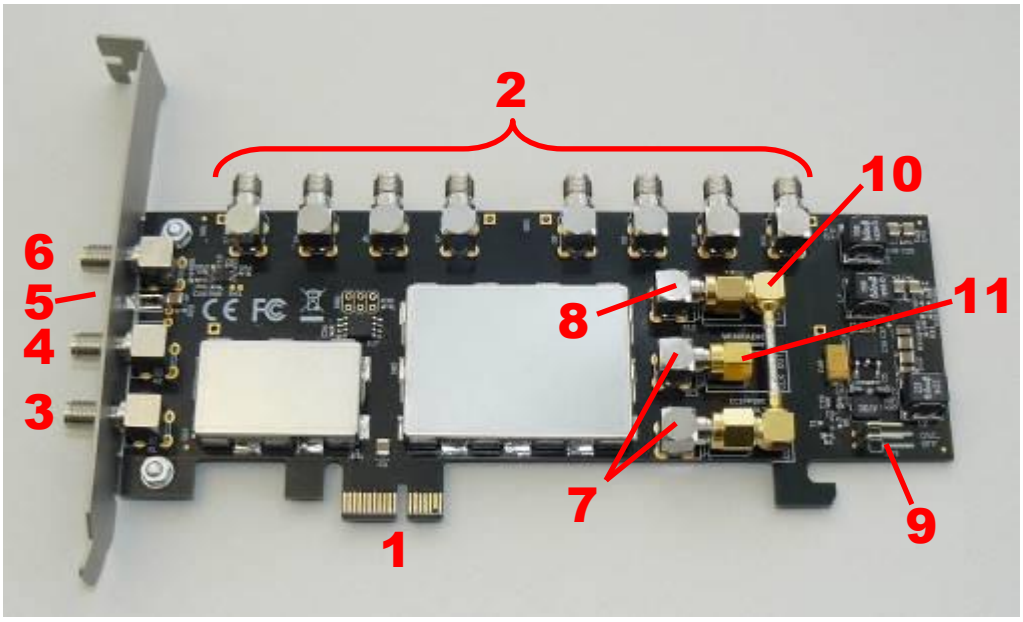
2.2.1 Coherent clock generator board

The Coherent clock generator board is shown in Picture 2-4. It is a PCIe card, which has to be installed into PCIe slot inside a PC. The board generates a 100 MHz sampling clock for up to eight WR-G35DDCi receivers. The sampling clock is locked to a frequency reference, which can be internal or external. It also can distribute a 1PPS trigger signal from the 1PPS input to the WR-G35DDCi receivers when used in a standard installation, but in the ETC configuration this feature is not utilized.

In the ETC configuration, this board has to be accompanied with additional hardware – the PCIe bracket multi-SMA adapter, described in Section 2.4. This hardware carries the clock signals generated by this board out of the PC chassis, so the sampling clock can be distributed to the receivers externally to the PC. As the sampling clock is distributed externally, there is no requirement for this card to be installed together with any of the WR-G35DDCi receivers in the ETC configuration.

No software driver is required for operation of the Coherent clock generator board.

For the technical specification of the board, please refer to chapter 5 of this document.



1 PCIe connector
2 SMA connectors for sampling clock output
3 Frequency reference output REF OUT
4 Frequency reference input REF IN
5 Locked indicator
6 1PPS trigger input – unused in ETC configuration
7 SMA connectors for local oscillator output
8 SMA connector for local oscillator input
9 Pin header for disabling the oscillator
10 Factory pre-installed SMA jumper
11 Factory pre-installed SMA terminator

Picture 2-4: Front view of the Coherent clock generator board with 1 PPS input

2.2.2 PCIe connector

The PCIe connector provides power to the Coherent clock generator board. As there is no data communication running through the PCIe connector, no software driver is required for proper operation of the board. However, the board must be installed into a PCIe slot inside of a PC.

2.2.3 SMA connectors for sampling clock output

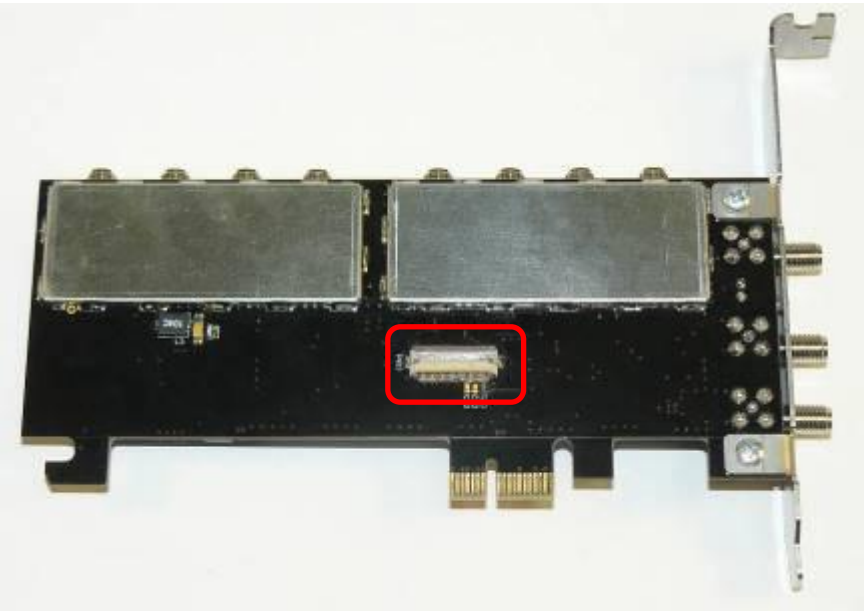
There are eight SMA connectors for the sampling clock output provided on the Coherent clock generator board. These are located on the top of the board and are facing upwards. Each WR-G35DDCi receiver within a coherent group must be connected to one of these ports using the SMA patch cables (for Coherent clock distribution) supplied with the Clock Kit and described in Section 2.2.9. All ports are equivalent; therefore, any receiver within a coherent group can be connected to any of these ports. However, unused ports have to be terminated using the 50 ohm SMA terminators for proper operation.

Because the sampling clock is distributed externally to the PC in the ETC configuration, extra hardware is needed to carry the clock signals out of the PC chassis. The PCIe bracket multi-SMA adapter described in chapter 2.4.

For the technical specification of the sampling clock output signal, please refer to Chapter 5.

2.2.4 Digital synchronization interface

The digital synchronization interface is located on the rear side of the board. It is unused in the ETC configuration and has to be left unconnected when operating in the ETC configuration.



Picture 2-5: Rear view of the Coherent clock generator board showing the location of the digital synchronization interface marked in red – it is unused and has to be left unconnected in the ETC configuration

2.2.5 Frequency reference output REF OUT

The frequency reference output is an SMA connector providing the 10 MHz (internally derived) frequency reference output signal. This output can be connected to the REF IN input port (Section 2.2.6) if the internal frequency reference operation of the board is required. Use the Frequency Reference SMA Interconnect cable (described in Section 2.2.12 and provided with the Clock Kit) to connect the REF OUT port to the REF IN port.

If unused, this port must be properly terminated using the 50 ohm terminator.

For the technical specification of the REF OUT, please refer to Chapter 5.

2.2.6 Frequency reference input REF IN

A signal provided to the frequency reference input REF IN serves as a frequency reference for the 100 MHz sampling clock generator. It is a 50 ohm terminated SMA connector. A 10 MHz reference signal must be provided on this input.

This input can be connected to the REF OUT output port (Section 2.2.5) if the internal frequency reference operation of the board is required. Use the Frequency Reference SMA Interconnect cable (described in Section 2.2.12 and provided with the Clock Kit) to connect the REF OUT port to the REF IN port.

For the technical specification of the REF IN input, please refer to Chapter 5.

2.2.7 1PPS trigger input

The 1PPS trigger input is unused in the ETC configuration and has to be left unconnected when operating in the ETC configuration.

2.2.8 Locked indicator

The ‘Locked’ indicator is lit whenever the 100 MHz sampling clock generator is locked to the frequency reference signal provided at the REF IN port. For more information about the REF IN port please refer to Section 2.2.6.

2.2.9 SMA patch cables for Coherent clock distribution

There are nine SMA patch cables (45 cm long) supplied with the Clock Kit. Eight of these cables are used in the ETC configuration to carry the sampling clock from the Coherent clock generator board to eight SMA adapters located on the PCI bracket SMA adapter; described in Section 2.4. The cable carries the clock signal out of the PC chassis to distribute it to all WR-G35DDCi receivers which are in coherent operation.

For interconnection, only use the original WiNRADiO SMA patch cables supplied with the Clock Kit as these are specially matched to be coherent.

Picture 2-6: WiNRADiO coherent SMA patch cable

2.2.10 Digital synchronization cables for each WR-G35DDCi receiver

There are eight digital synchronization cables supplied with the Clock Kit. These are unused in the ETC configuration, therefore do not install them. However, these cables should be kept safely, in case the Clock Kit is required to operate in standard (non-ETC) coherent receiver operation in the future.

Picture 2-7: Digital synchronization cable for the WR-G35DDCi receiver, unused in the ETC configuration (see text)

2.2.11 Digital synchronization cable for the Coherent clock generator board

Similar to the digital synchronization cables described in the previous Section, this cable is unused in the ETC configuration, therefore do not install this cable. However, this cable should be kept safely, in case the Clock Kit is required to operate in standard (non-ETC) coherent receiver operation in the future.

Picture 2-8: Digital synchronization cable for the Coherent clock generator board, unused in the ETC configuration (see text)

2.2.12 Frequency reference SMA interconnect cable

The frequency reference SMA interconnect cable is used to interconnect the internal reference output REF OUT of the Coherent clock generator board to the frequency reference input REF IN of the same board, after it is installed into a PC. If an external frequency reference is used, this cable is not needed and should be kept safely, in case the internal reference operation is required in the future.

For installation of the cable please refer to chapter 3 of this document.

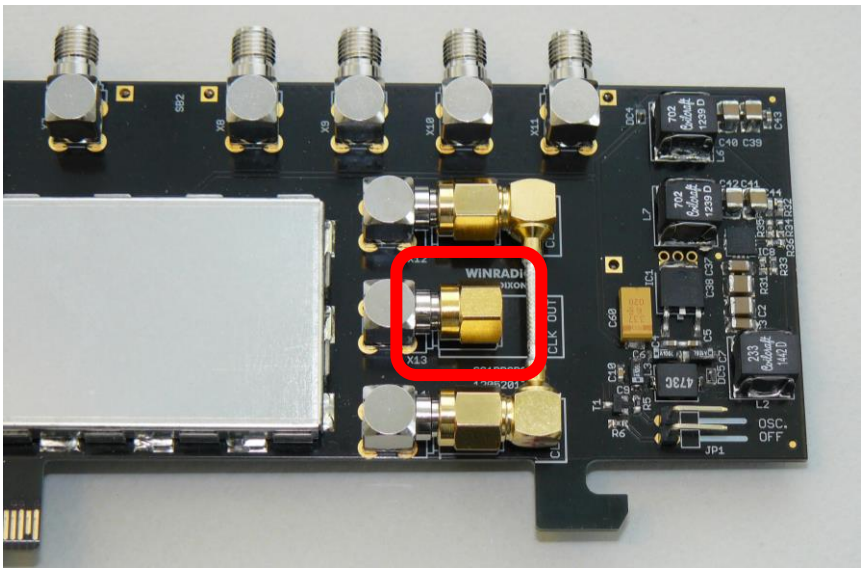
Picture 2-9: SMA interconnect cable for the frequency reference

2.2.13 SMA terminators

The Clock Kit comes with eight 50 ohm SMA terminators. These terminators must occupy all unused sampling clock outputs on the Coherent clock generator board. If all sampling clock outputs on the Coherent clock generator board are connected to the 'PCIe bracket multi-SMA adapter' (as described in Section 2.4) and some of the outputs on the PCI bracket SMA adapter are unused, all these unused outputs must have terminators installed on them. A minimum of two WR-G35DDCi receivers can be connected as a coherent pair, so six terminators are needed to terminate the sampling clock outputs. A seventh terminator is provided in case the external reference is used with the Coherent clock generator board. In such a case, the terminator must be installed on the REF OUT port of the Coherent clock generator board.

Picture 2-10: SMA terminators

The eighth terminator comes factory pre-installed on the Coherent clock generator board, terminating the secondary sampling clock oscillator output as shown in picture 2-11.



Picture 2-11: SMA terminator (marked in red) are factory pre-installed on the secondary sampling clock oscillator output

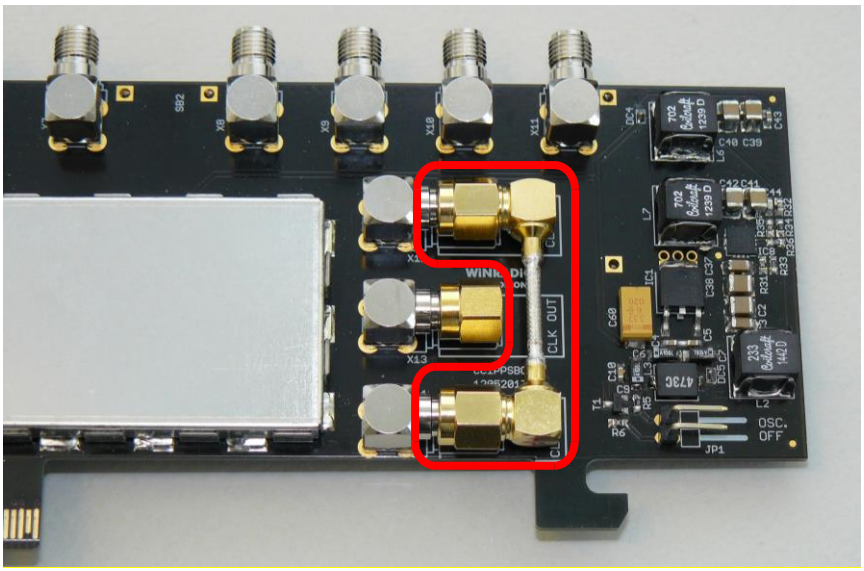
2.2.14 Sampling clock oscillator input and outputs

The Coherent clock generator board has two sampling clock oscillator outputs and one input for the sampling clock oscillator. These are factory connected as shown in Picture 2-12 using an SMA jumper cable as described in Section 2.2.15, and one SMA 50 ohm terminator.

These factory connections need not to be altered for normal operation when using the Coherent clock generator board to drive up to eight coherent receivers.

The purpose of these connectors is to enable the use of **two Coherent clock generator boards** to coherently drive up to sixteen receivers. For details on how to use two Coherent clock generator boards (to drive up to sixteen receivers) please refer to chapter 4 of this document.

The factory connections consists of one 50 ohm terminator installed on one of the sampling clock outputs and an SMA jumper cable as described in Section 2.2.15. This interconnects the sampling clock, from the sampling clock oscillator output to the input of the sampling clock oscillator.



Picture 2-12: Factory pre-installed SMA jumper cable interconnecting (marked in red) the primary sampling clock oscillator output with the sampling clock oscillator input. Please note the mandatory terminator installed on the secondary sampling clock oscillator output.

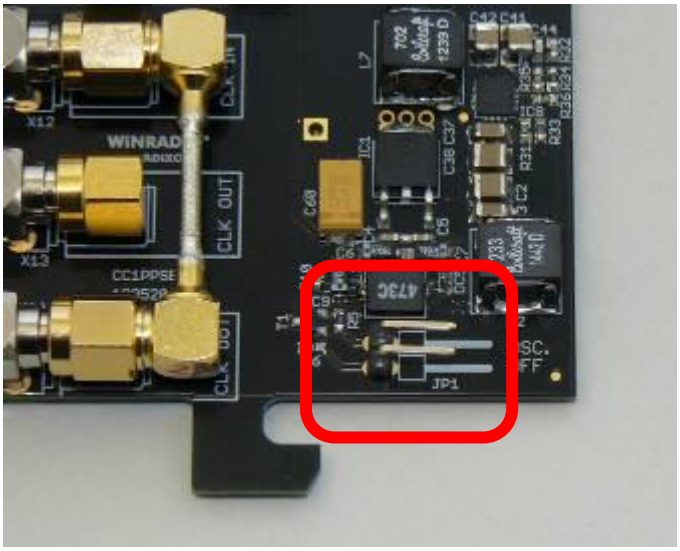
2.2.15 SMA jumper cable

The Clock Kit comes with an SMA jumper cable to connect the primary sampling clock oscillator output to the sampling clock oscillator output. This SMA jumper is factory pre-installed and is shown in picture 2-12. The jumper must be replaced with a proper patch cable when using two Coherent clock generator boards, to distribute the sampling clock to up to sixteen receivers. For details on how to use two Coherent clock generator boards (to drive up to sixteen receivers) please refer to chapter 4 of this document.

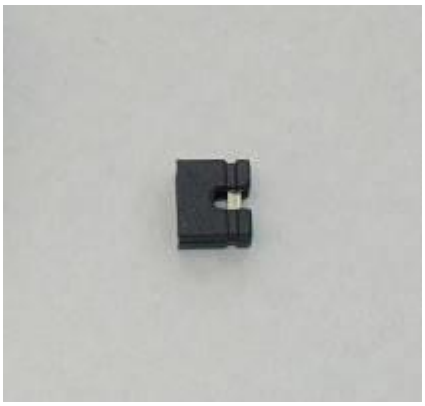
2.2.16 Pin header for disabling the sampling clock oscillator

The 'pin header' for disabling the sampling oscillator is shown in picture 2-13 with its corresponding jumper is shown in picture 2-14. No jumper is installed on the header for normal operation of a single Coherent clock generator board.

The purpose of the pin header and its corresponding jumper is to provide the ability to turn off the local sampling clock oscillator on one of the Coherent clock generator boards when two Coherent clock generator boards are used to coherently drive up to sixteen receivers. For details on how to use two Coherent clock generator boards (to drive up to sixteen receivers) please refer to chapter 4 of this document.



Picture 2-13: Pin header for disabling the sampling clock oscillator (marked in red)



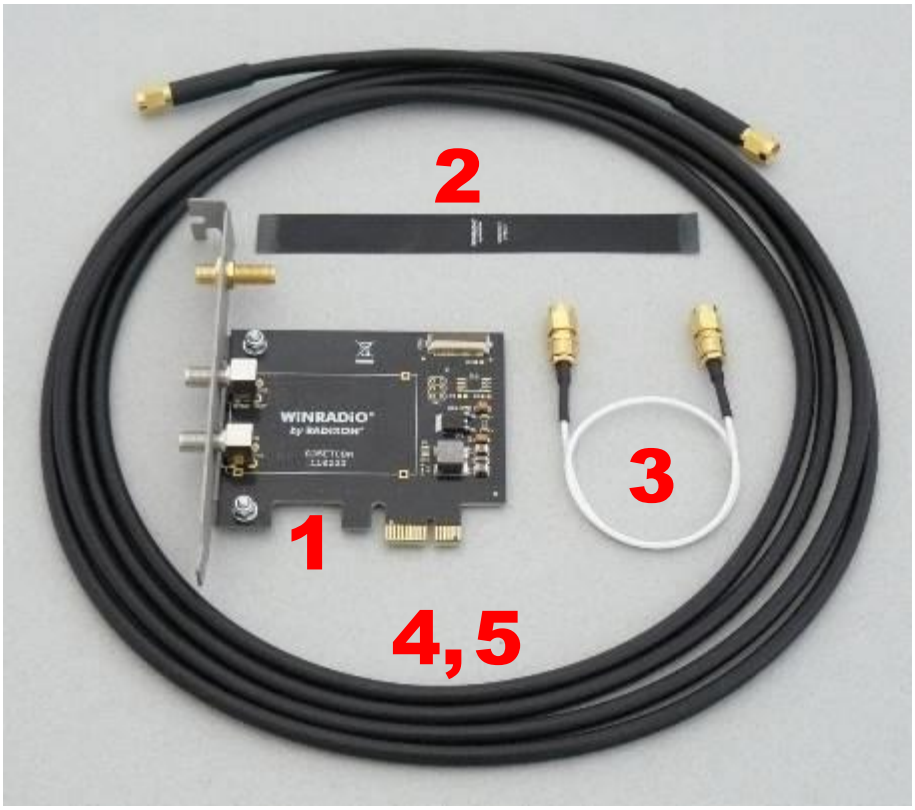
Picture 2-14: Jumper for disabling the sampling clock oscillator

2.3 The WiNRADiO ETC kit (WR-ETC-100)

The 'WiNRADiO ETC kit' (hereafter referred to as the 'ETC Kit') provides coherent synchronization capability between multiple WR-G35DDCi receivers operating in ETC mode. A single ETC kit is needed for each WR-G35DDCi receiver. In other words, the number of required ETC kits is equal to the number of coherent receivers.

The ETC kit converts coherent synchronization signals from the Digital synchronization connector of the WR-G35DDCi (described in Section 2.1 and shown in the Picture 2-2) into signals carried over standard 50 ohm coaxial SMA cables. This enables the receivers to be installed while distributed in different PCs. The ETC Kit consists of the following components (shown in Picture 2-15):

1. The Extended topology configuration board (ETC board)
2. Digital synchronization cable for the ETC board
3. The 30 cm SMA sampling clock patch cable
4. The CLOCK SMA coaxial cable for external connections of the sampling clock
5. The SYNC SMA coaxial cable for external connections of synchronization



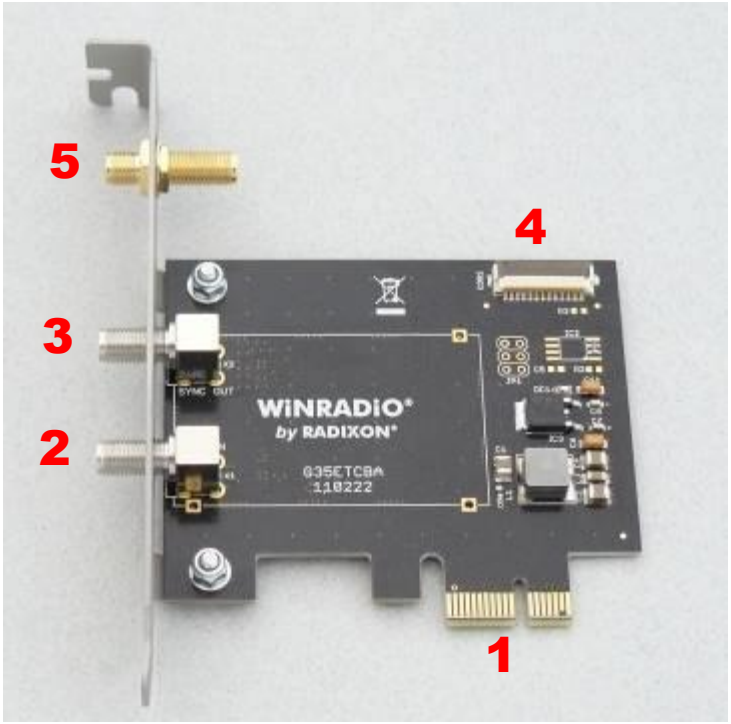
Picture 2-15: The WiNRADiO ETC kit (WR-ETC-100) and its components

2.3.1 ETC kit board

The ETC board is shown in Picture 2-16. This is a PCIe card, which has to be installed into a PC, next to and connected to each WR-G35DDCi receiver; one ETC board is required for each receiver. The board receives synchronization signal from the previous receiver in the synchronization chain through the SYNC IN connector and re-sends it to the next receiver in the chain through the SYNC OUT connector. The SYNC IN connector on the first-in-chain board can be left unconnected, or it can be used to supply the 1PPS signal when time-stamping functionality is required. The SYNC OUT connector on the last-in-chain board has to be left unconnected.

No software driver is required for operation of the ETC board.

For the technical specification of the board, please refer to chapter 5 of this document.



1 PCIe connector

2 SMA connector SYNC IN for the synchronization signal input

3 SMA connector SYNC OUT for the synchronization signal output

4 Digital synchronization interface for connection to the WR-G35DDCi receiver

5 SMA adapter for the sampling clock

Picture 2-16: The ETC kit board

2.3.2 PCIe connector

The PCIe connector provides power to the ETC board. As there is no data communication running through the PCIe connector, no software driver is required for proper operation of the board. However, the board must be installed into a PCIe slot inside of a PC.

2.3.3 SMA connector SYNC IN

The purpose of the SYNC IN connector is to receive the synchronization signal from the preceding ETC card in the synchronization chain. Therefore, the SYNC IN connector has to be connected to the SYNC OUT connector of the preceding ETC board in the synchronization chain. To facilitate this connection, the SMA synchronization coaxial cable (the SYNC cable) described in Section 2.3.9 is used.

The SYNC IN connector on the first-in-chain board can be left unconnected. Alternatively, it can be used as the input for the 1PPS signal, when timestamping functionality is required.

The synchronization protocol utilized on this interface is proprietary to WiNRADiO, therefore no further specification is provided.

2.3.4 SMA connector SYNC OUT

The purpose of the SYNC OUT connector is to transmit the synchronization signal to the receiver next in the synchronization chain. Therefore, the SYNC OUT connector has to be connected to SYNC IN connector of the ETC board which follows it in the synchronization chain. To facilitate this connection, the SMA synchronization coaxial cable (the SYNC cable) described in Section 2.3.9 is used.

The SYNC OUT connector on the last-in-chain board has to be left unconnected.

The synchronization protocol utilized on this interface is proprietary to WiNRADiO, therefore no further specification is provided.

2.3.5 Digital synchronization interface

The digital synchronization interface of the ETC board transfers synchronization signals between the ETC board and the receiver. The digital synchronization cable for the ETC board (described in Section 2.3.7) attaches to this connector and provides a connection to the digital synchronization connector of the receiver (described in Section 2.1 and shown in the Picture 2-2).

The synchronization protocol utilized on this interface is proprietary to WiNRADiO, therefore no further specification is provided.

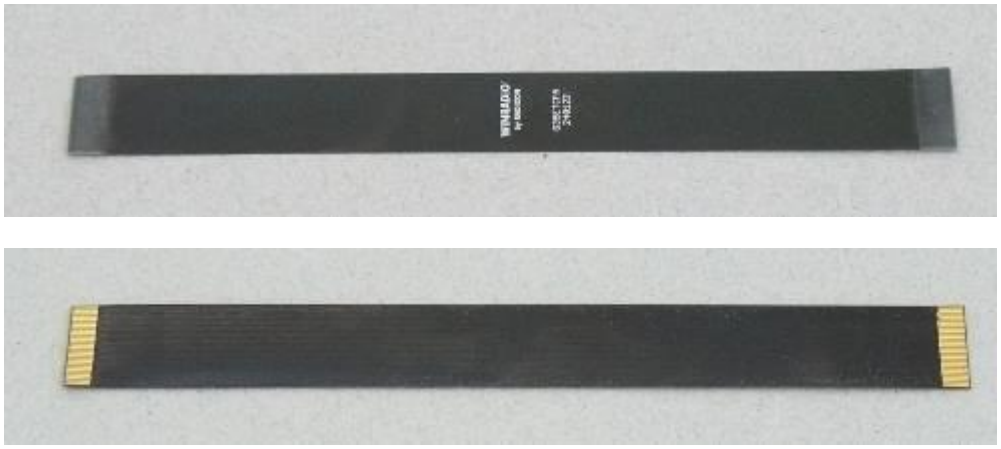
2.3.6 SMA adapter for the sampling clock

The SMA adapter for the sampling clock allows for entrance of the sampling clock to the PC chassis interior. In ETC configuration, all connections between receivers and the Coherent clock generator board (see Section 2.2.1) are done externally to the chassis of the PCs. However, the Coherent clock input of the receiver shown in Picture 2-1 is located on the receiver, which is installed inside the PC chassis. This SMA adapter passes the sampling clock from the PC chassis - exterior to interior. Externally to the PC chassis, this SMA adapter is connected to the Coherent clock generator board's clock output. Internally, the 30 cm SMA patch cable supplied with the ETC kit (Section 2.3) is used to carry the sampling clock from the SMA adapter to the Coherent clock input of the receiver (shown in Picture 2-1).

2.3.7 Digital synchronization cable for ETC board

The digital synchronization flat cable for the ETC board provides connection between the digital synchronization connector of the ETC board (described in Section 2.3.1) and the digital synchronization connector of the receiver (described in Section 2.1 and shown in the Picture 2-2).

The cable is fully reversible, i.e. there is no requirement to install a specific end of the cable to the specific board. Therefore, the orientation of the cable is arbitrary when installing the cable.



Picture 2-17: The Digital synchronization flat cable for the ETC board front view (top) and back view (bottom)

2.3.8 30 cm SMA sampling clock patch cable

The 30 cm SMA sampling clock patch cable is shown in Picture 2-18. It connects between the SMA adapter for the sampling clock described in Section 2.3.6 and the sampling clock input of the receiver shown in Picture 2-1. Its purpose is to carry the sampling clock from the exterior of the PC to the receiver.

For interconnection, **only use the original WiNRADiO 30 cm SMA sampling clock patch cable** supplied with the ETC Kit, as it is specially matched to be coherent.

Picture 2-18: The 30 cm SMA sampling clock patch cable

2.3.9 SMA coaxial cables for external connection of the sampling clock and synchronization

There are two long SMA coaxial cables supplied with the ETC Kit (shown in the Picture 2-19). Both cables are almost identical, but differ in purpose and connection. The cables are distinguished by a labelled sticker attached to them.

First cable is called the **CLOCK CABLE** (see Picture 2-19 and 2-20 on the left) and is used to distribute the sampling clock from the Coherent clock generator board of the Clock Kit to all WR-G35DDCi receivers which are in the coherent group.

The other cable is called the **SYNC CABLE** (see Picture 2-19 and 2-20 on the right) and is used to link the receivers in a daisy chain like manner, to synchronize the receivers for coherent operation. Each SYNC CABLE has the delay value specified on its sticker. The delay value is marked as "DELAY n CLK" where 'n' is an integer number, which specifies the amount of sampling clock cycles by which the cable delays the signal.

These cables can be manufactured in various lengths; however, the length is not arbitrary. As mentioned above, the length of the cable is marked on the sticker of the SYNC CABLE in by the number of sampling clock cycles which it delays the signal. Shortest cable has a delay of 2 sampling clock cycles and is approx. 0.8 metres long. The longer cable has a delay of 3 sampling clock cycles and is approx. 2.8 metres long. If longer cables are needed, please contact WiNRADiO.

All cables used for coherent operation of receivers must be the same length and type in the ETC configuration. Cables of various length and/or types cannot be mixed within one coherent group of receivers. Also, the user must specify the delay of the SYNC CABLE in the software, so the software can compensate for the delay.

The delay is specified by the number of sampling clock cycles which it delays the synchronization signal and is recorded on the label of each SYNC CABLE in the last row, see the Picture 2-20 on the right.

For interconnection, **only use the original WiNRADiO SMA patch cables supplied with the ETC Kit as these are specially matched to be coherent**. Do not mix different cable lengths or different cable types.

Picture 2-19: The SMA coaxial cable for external connection of the sampling clock (the CLOCK cable). The SMA coaxial cable for the external connection of synchronization (the SYNC cable) is identical to the CLOCK cable.
The cables are distinguished by a label attached to them, see Picture 2-20.

Picture 2-20: Note the labels of the CLOCK SMA coaxial cable (on the left) and of the SYNC SMA coaxial cable (on the right) supplied with the ETC kit. The DELAY specification is stated on the SYNC cable shown on the right – this particular cable shown in the picture has the delay specified as "DELAY 3 CLK". That means the cable delays the signal by 3 sampling clock periods. The value of the delay has to be specified in the software, so that the software can compensate for the delay.

2.4 The WiNRADiO PCIe Bracket Multi-SMA Adapter

The WiNRADiO 'PCIe Bracket Multi-SMA Adapter' consists of eight SMA to SMA connector adapters mounted on a standard PCI bracket. It is designed to be installed into a standard PCIe card position slot inside a PC chassis. Its purpose is to provide SMA connection between the interior and exterior of a PC chassis for eight coherent sampling clock signals from the Coherent clock generator board (described in Section 2.2.1) in the ETC configuration.

In ETC configuration, this multi-SMA adapter is installed in the same PC chassis as the Coherent clock generator board, into a PCI/PCIe position next to it. It is connected to eight sampling clock outputs of the Coherent clock generator board using eight SMA patch cables of the Clock Kit (see the Section 2.2.9). This way, the Coherent clock signals generated by the Coherent clock generator are carried out of the PC chassis, so the sampling clock can be distributed to coherent receivers externally, outside of the PC, using the CLOCK SMA coaxial cables for external connections of sampling clock described in Section 2.3.4.

Picture 2-21: The PCI bracket multi-SMA adapter

3. ETC installation of up to eight receivers

The basic setup of up to eight receivers in the ETC configuration is shown in Picture 3-1, although only four receivers are shown in the picture for the picture clarity. A simplified version of an eight channel setup is shown in the Picture 3-2.

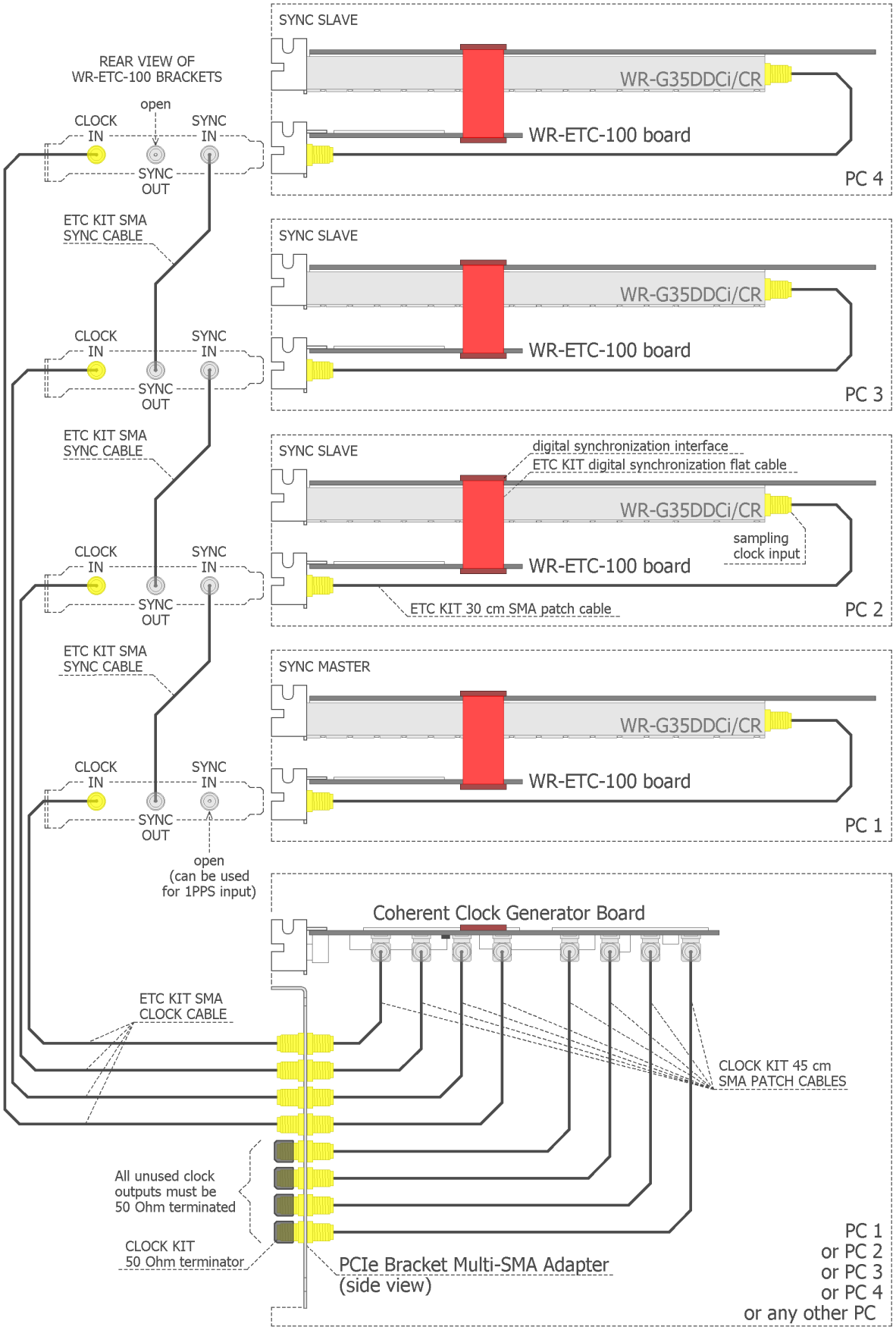
The setup consists of a minimum two and up to eight WR-G35DDCi receivers, each installed into a PCIe slot inside separate PCs. Each receiver must be accompanied by its own dedicated ETC kit (described in Section 2.3) installed into a PCIe slot of the same PC as the particular receiver. In other words, the number of ETC kits needed is equal to the number of receivers installed. The ETC kit allows for the external interconnections needed for coherent operation in the ETC configuration.

As mentioned above, in the ETC configuration, each WR-G35DDCi receiver is typically installed in a separate dedicated PC. Installation of multiple receivers inside the same PC is allowed in the ETC configuration, however each receiver has to be accompanied with its own dedicated ETC card. Also, the receivers installed inside the same PC act the same way, as if they were installed in separate dedicated PCs. In other words, all interconnections have to be done externally through the ETC board and each receiver has to run its own instance of software. Also, it is not possible to mix the ETC installation (i.e. external interconnections, described in this document) with the standard installation (i.e. internal interconnections, described in another document). All interconnections have to be done externally through the ETC board, outside of the PC, even if two or more receivers are installed in the same PC.

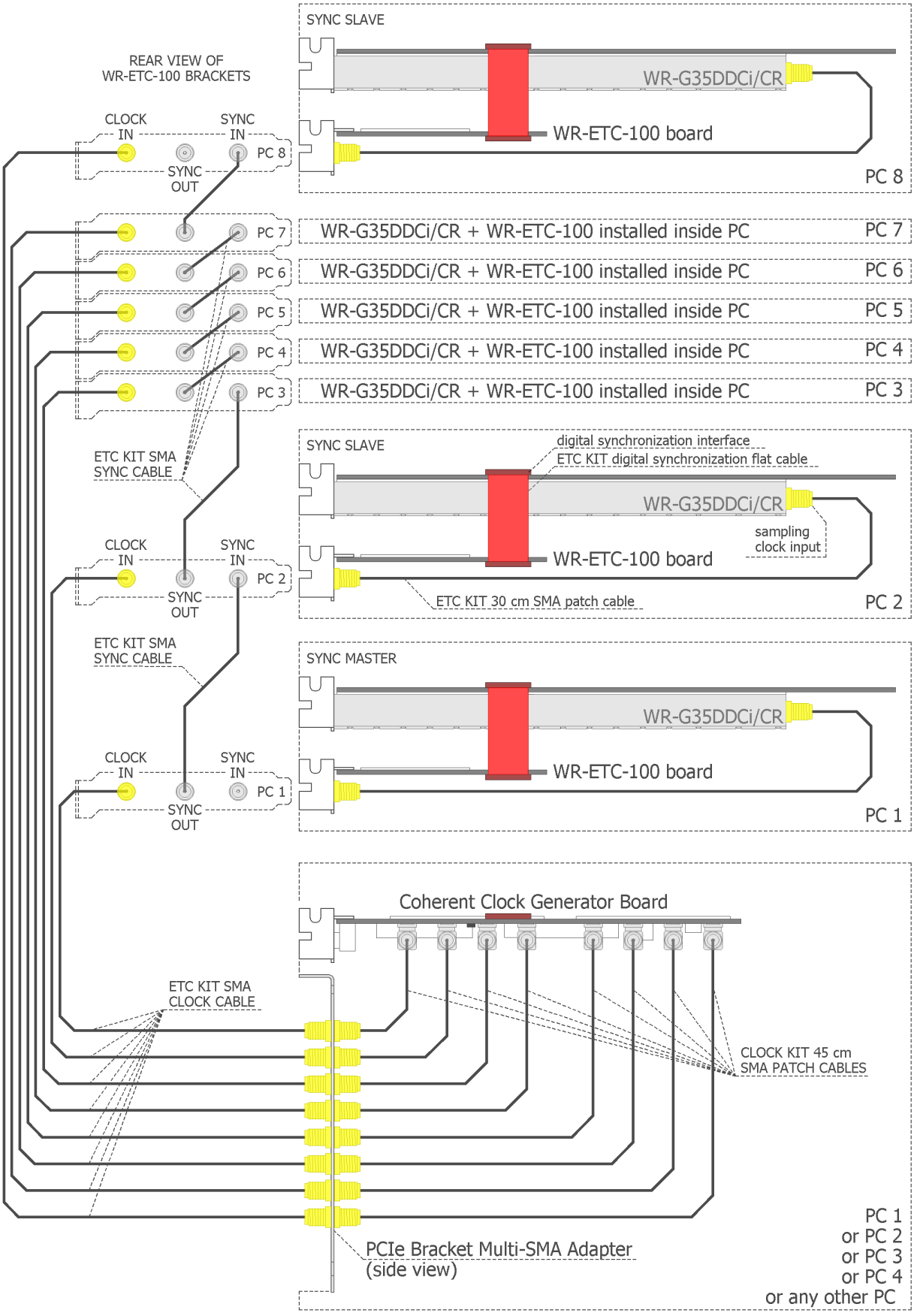
Another part of the setup is the Coherent clock Generator Board of the Clock Kit (described in Section 2.2), which generates eight coherent sampling clock signals for the receivers. The Clock Board has to be installed into a PCIe slot inside of a PC. The choice of the PC for the installation of the Clock Board is arbitrary. There is no requirement for the Clock Board to be installed in a specific PC. It can be installed into a PC together with any receiver it feeds, but doesn’t have to be installed together with any receiver at all. It can (but doesn’t have to) be installed in separate PC, if desired.

The Coherent clock Generator Board must be accompanied by the ‘PCIe bracket multi-SMA adapter’ described in Section 2.4 (and therefore installed inside the same PC), which allows for external interconnections of the coherent sampling clock signals generated by the Coherent clock Generator Board.

The receivers and the Coherent Clock Generator Board are interconnected using two types of cables – the CLOCK cable and the SYNC cable (described in Section 2.3.9). The CLOCK cables distribute the sampling clock and connect between the Coherent Clock Generator Board and each receiver. The SYNC cables distribute the synchronization signals needed to synchronize the receivers for coherent operation and are connected between neighbouring receivers in a daisy-chain like manner. The receiver connected first in the synchronization chain (shown installed in PC1 in Picture 3-1) generates the synchronization signals and is called the synchronization master (SYNC MASTER). The other receivers receive and re-transmit the synchronization signals and are called synchronization slaves (SYNC SLAVE).



Picture 3-1: Sampling clock and digital sync signal interconnection of four WR-G35DDCi/CR receivers in ETC configuration.



Picture 3-2: Sampling clock and synchronization interconnection of eight WR-G35DDCi/CR receivers in ETC configuration. Channels 3 to 7 are identical to channels 1,2 and 8.

3.1 Preparing the receivers for installation into a PC

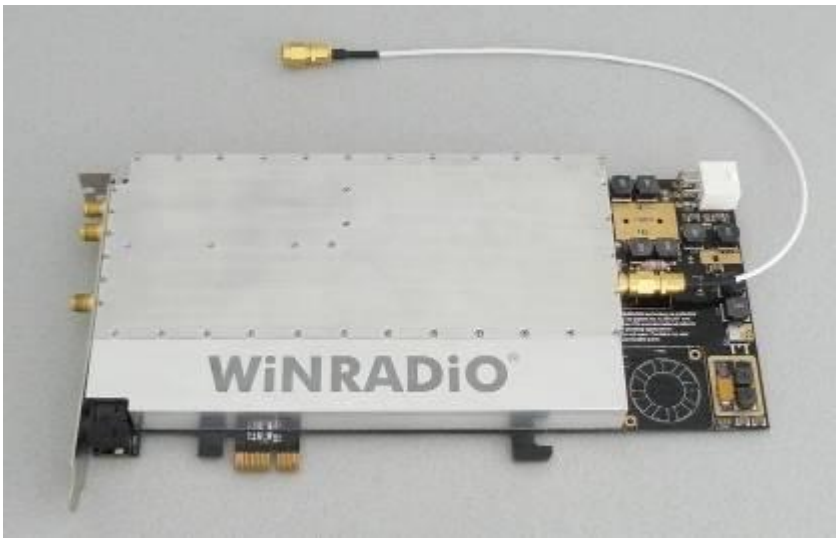
Prior to installation into a PC, attach the 30 cm SMA sampling clock patch cable of the ETC kit (described in Section 2.3.8) to the Coherent clock input of each receiver, leaving the other end of cable unconnected for now. The Coherent clock input of the receiver is shown in Picture 2-1.

Please refer to Picture 3-3 for installation details.

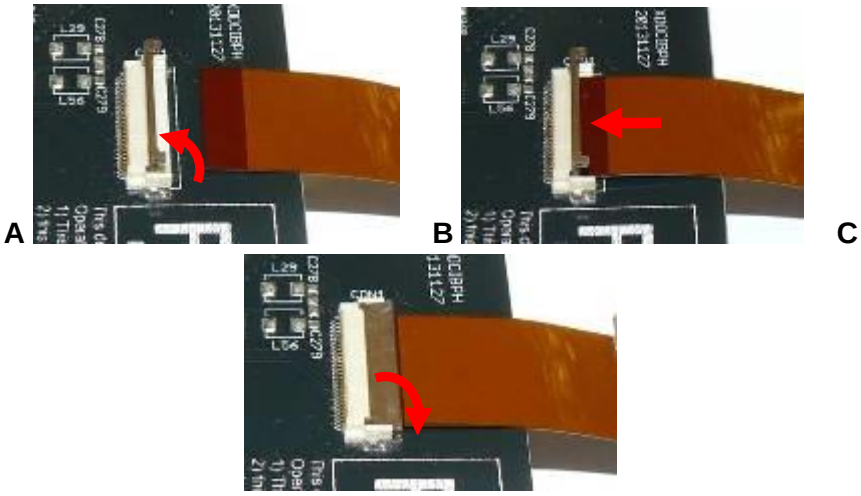
Also prior to installation into a PC, please attach the Digital synchronization cable for ETC board described in Section 2.3.7 to the digital synchronization port of each WR-G35DDCi receiver, also leaving the other end of cable unconnected for now.

The digital synchronization interface connector is shown in Picture 2-2. Please refer to Picture 3-5 for installation details. The cable is fully reversible, i.e. there is no requirement to install specific end of the cable. Either end of the cable can be installed into the receiver. For FPC (Flat Printed-circuit Cable) connector installation instructions, please refer to Picture 3-4.

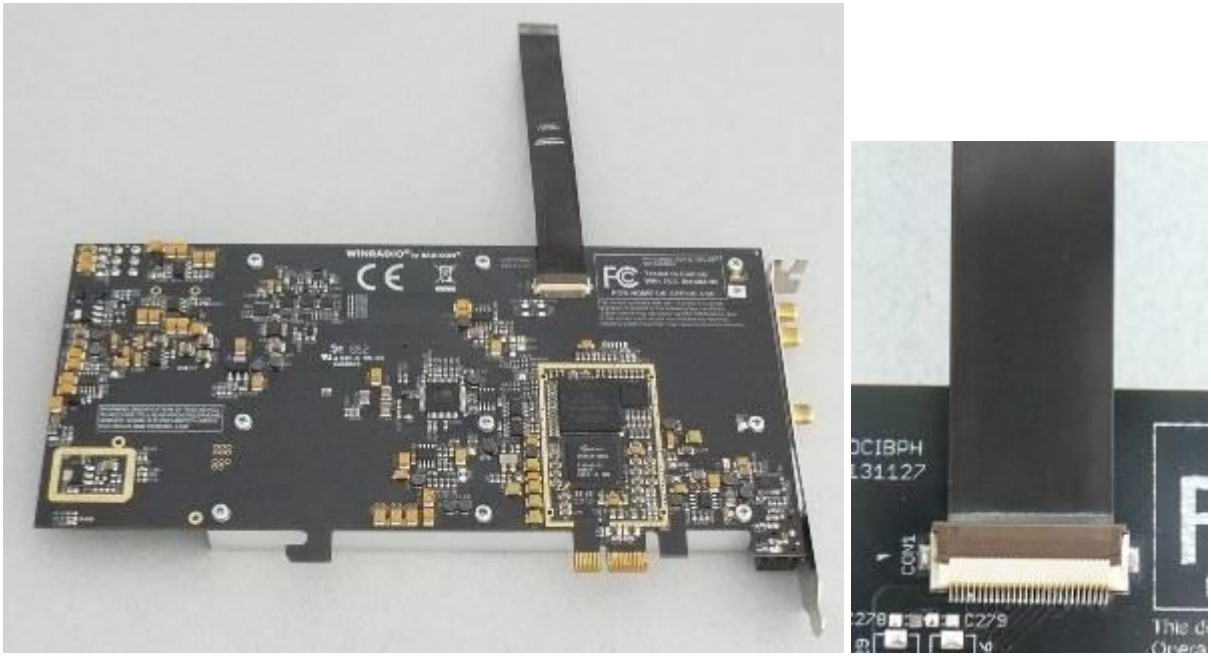
These two steps should be performed for each WR-G35DDCi receiver prior to installation into a PC because the Coherent clock input and the digital synchronization port of each receiver are more difficult to access after the receiver has been installed into a PC.



Picture 3-3: Sampling clock patch cable installed onto a receiver



Picture 3-4: Installing the FPC connector
(for clarity, the cable shown here is of another color)



Picture 3-5: Digital synchronization cable installed to a receiver. The cable orientation is arbitrary, either end of the cable can be installed to the connector of the receiver.

3.2 Installing the receiver into a PC

A PC has to be powered off when installing the receiver into a PCIe slot.

Each receiver has to be prepared for installation as discussed in Section 3.1.

As mentioned earlier, in the ETC configuration, each WR-G35DDCi receiver is typically installed in a separate dedicated PC. Each receiver must be accompanied with its own dedicated ETC card. Therefore, two PCIe slots are needed for installation of each receiver – one PCIe slot for the receiver and one PCIe slot for the ETC card. The ETC card is typically installed into a slot next to the receiver and is described in next Section 3.3.

Installation of multiple receivers inside the same PC is allowed in the ETC configuration, however each receiver has to be accompanied with its own dedicated ETC card. Therefore, the number of PCIe slots required for the installation is twice the number of receivers installed.

As shown in Picture 3-1, install the receiver into a PCIe slot of the PC, leaving the other ends of both the sampling clock cable and the digital synchronization cable unconnected. Leave at least one PCIe slot empty next to the receiver to allow for installation of the ETC board.

For details of receiver installation into a PC PCIe slot, please refer to the WR-G35DDCi user guide.

Picture 3-6: A receiver is installed into the PC, showing other ends of the flat synchronization cable and SMA coaxial clock cables unconnected.

3.3 Installing the ETC board into the PC

As mentioned in the previous step, the PC has to be powered off when installing the ETC board into a PCIe slot.

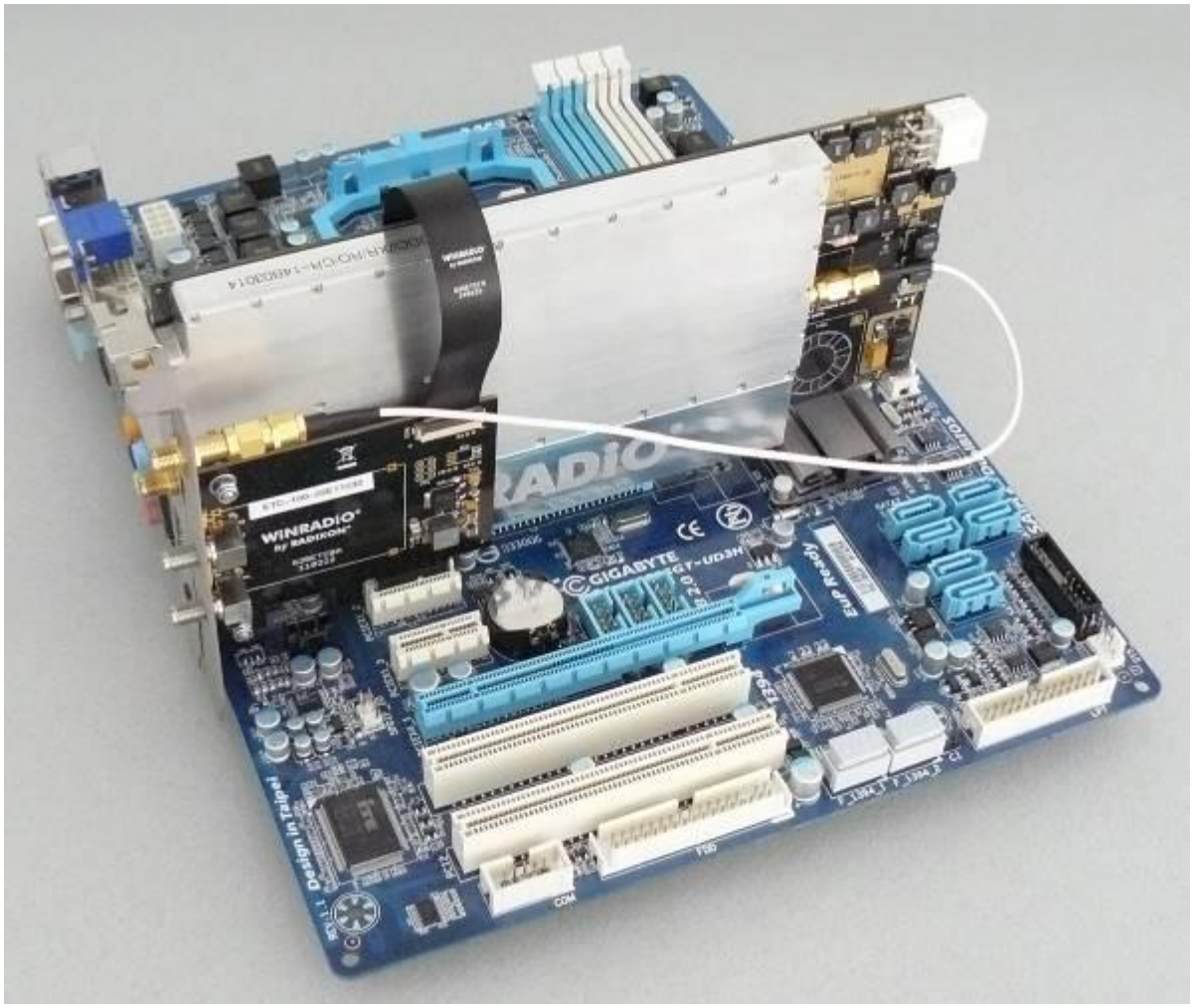
Prior to inserting the ETC card into a PCIe slot, interconnect the ETC card to the receiver which is already installed in PC, as described in previous Section.

Firstly, connect the loose end of the flat synchronization cable (which is already connected to the receiver) to the flat cable connector of the ETC board as show in Picture 3-7 (1). For the FPC (Flat Printed-circuit Cable) connector installation instructions, please refer to Picture 3-4.

Secondly, connect the loose end of the 30 cm SMA clock patch cable (which is already connected to the receiver) to the sampling clock SMA adapter located on the bracket of the ETC card as show in Picture 3-7 (2).

Finally, carefully insert the ETC card into the PCIe slot next to the receiver, as shown in the Picture 3-8.

Picture 3-7: Prior to inserting the ETC card into a PCIe slot, first connect the flat synchronization cable to the flat cable connector (1) of the ETC card, and then connect the SMA sampling clock patch cable to the sampling clock SMA adapter (2) of the ETC card.



Picture 3-8: The completed installation of the ETC board into the PC next to the receiver.

Picture 3-9: The completed installation of the receiver (shown on the left) and the ETC board (shown on the right) fitted into the PC as seen from the rear of the PC.

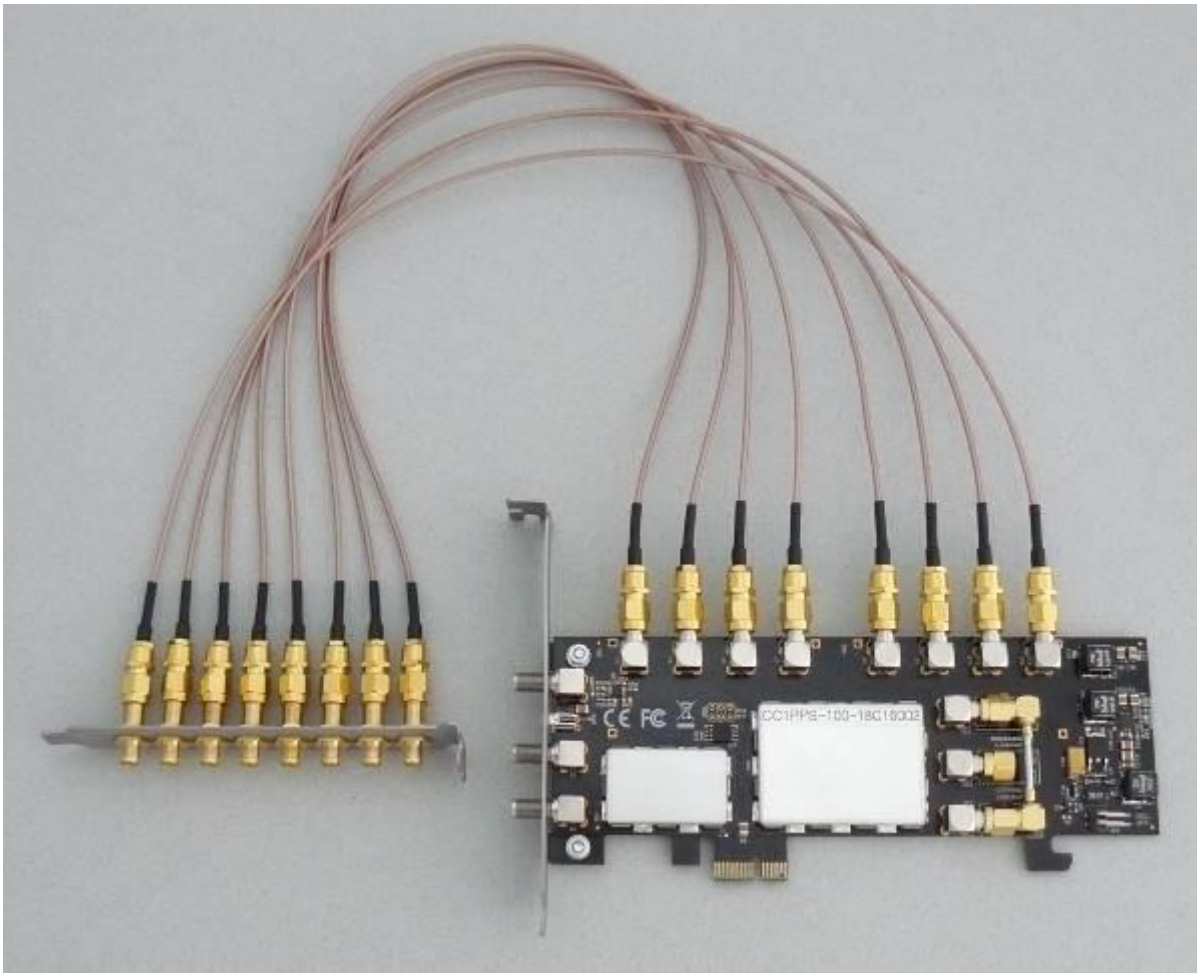
3.4 Interconnecting the Coherent Clock Generator board with the PCIe bracket multi-SMA adapter

Prior to installation of the Coherent clock generator board (described in Section 2.2.1) into the PC, interconnect the Coherent Clock Generator board with the PCIe bracket multi-SMA adapter (described in Section 2.4) using eight SMA patch cables supplied with the Clock Kit described in Section 2.2.9. The example of such interconnection is shown in the Picture 3-10.

The purpose of the PCIe Bracket Multi-SMA Adapter is to provide an SMA connection between the interior and exterior of the PC chassis, to feed eight coherent sampling clock signals from the Coherent clock generator board. This way the Coherent clock signals (generated by the Coherent clock generator) are carried out of the PC chassis, allowing the sampling clock to be distributed to coherent receivers externally, outside the PC. The CLOCK SMA coaxial cables are used for the external connections of the sampling clock described in Section 2.3.4.

There is no need to connect any particular sampling clock output of the Clock Board to any specific position on the PCIe Bracket multi-SMA Adapter. The connection order can be arbitrary. However, it is recommended, that all eight outputs of the Clock Board are interconnected with the eight SMA adapters of the PCIe Bracket multi-SMA Adapter, even if less than eight receivers are to be connected to the Clock board through the PCIe Bracket multi-SMA adapter. **All unused clock outputs of the PCIe bracket multi-SMA adapter have to be terminated using 50 ohm terminators** installed externally onto the multi-SMA adapter for proper operation as shown in Picture 3-1. This picture shows just four clock outputs are utilized and the other four ports are unused, so that the unused ports are terminated using 50 ohm terminators.

If you choose not to connect all eight outputs of the Clock Board to the PCIe Bracket multi-SMA Adapter, the 50 ohm termination has to be attached directly to each unconnected clock output on the Clock board to achieve correct operation.



Picture 3-10: This is an example of interconnection of the Coherent Clock Generator board of the Clock Kit with the PCIe bracket multi-SMA adapter. Interconnection is made using 45 cm SMA patch cables of the Clock kit. This interconnection is also shown schematically as a part of Picture 3-1 and Picture 3-2.

3.5 Installing the Coherent clock generator board into the PC

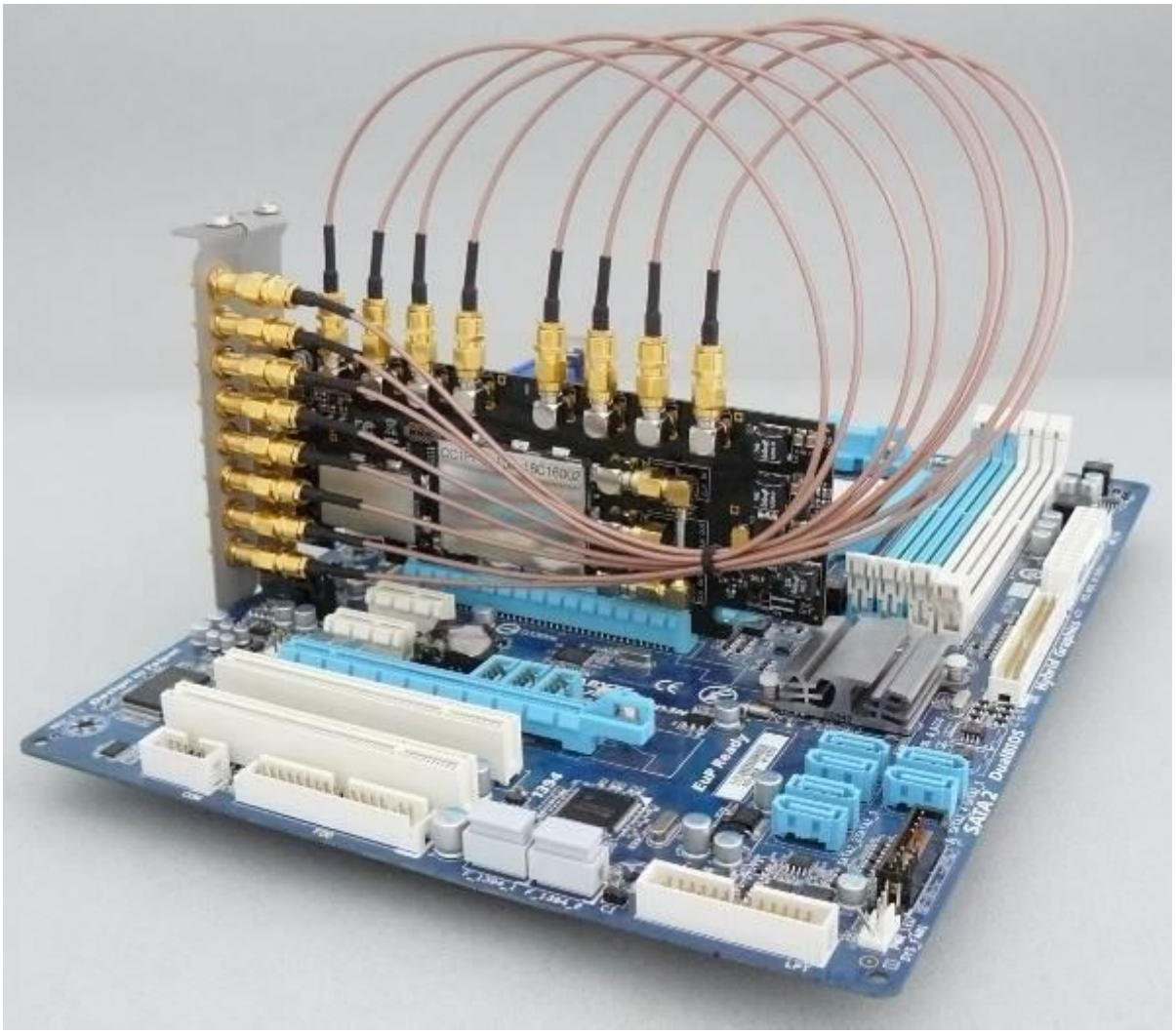
The PC has to be powered off when installing the Coherent clock generator board into a PCIe slot.

The Coherent clock generator board has to be prepared for installation by interconnecting it with the PCIe bracket multi-SMA adapter as described in the previous Section. The 1PPS input and digital synchronization interface of the Clock board are unused in the ETC configuration, no other preparation to the Clock Board is necessary in the ETC configuration.

The Clock Board has to be installed into a PCIe slot inside of a PC. However, in the ETC configuration, each WR-G35DDCi receiver is typically installed in a separate dedicated PC, therefore the complete setup consists of multiple PCs, in each PC the receivers together with ETC kits are installed. The choice of the PC for the installation of the Clock Board is arbitrary.

There is no requirement for the Clock Board to be installed in a specific PC. It can be installed in a PC together with any receiver it feeds, but doesn't have to be installed together with any receiver at all. It can (but doesn't have to) be installed in separate PC, if desired.

Start by installing the Clock Board into a PCIe slot of the PC. Next, install the PCIe Bracket multi-SMA adapter into a position next to the Clock Board. As the PCIe bracket multi-SMA interface is a passive device, it can be installed into any suitable position in the PC chassis, independent of the availability and type of the actual PC slot. Completed installation is shown in the Pictures 3-11 and 3-12.



Picture 3-11: The completed installation of the Coherent Clock Generator board into the PC together with the PCIe bracket multi-SMA adapter installed next to the Clock Board.

Picture 3-12: The completed installation of the Coherent Clock Generator board (on the left) into the PC together with the PCIe bracket multi-SMA adapter (on the right) installed next to the Clock Board as viewed from the rear side of a PC.

3.6 Choosing the frequency reference

When using the internal frequency reference, please connect the internal reference output REF OUT of the Coherent clock generator board to the frequency reference input REF IN of the Coherent clock generator board, after it has been installed into a PC (as shown in Picture 3-13). Please use the Frequency reference SMA interconnect cable as described in Section 2.2.12.

Picture 3-13: Installing the frequency reference SMA interconnect cable for internal frequency operation

When use of an external frequency reference is required, please connect the frequency reference signal to the REF IN port of the Coherent clock generator board as described in Section 2.2.6. Please note that the REF OUT port has to be properly terminated using the 50 ohm terminator when unused.

3.7 Connecting the CLOCK interconnection

The CLOCK interconnection is made externally, outside the PCs, between the Clock Board described in Section 2.2.1 and each receiver.

At the Clock Board side, this connection is made through the dedicated PCIe Bracket multi-SMA Adapter connected to the Clock Board as described in Section 3.4. The Clock Board with its dedicated PCIe Bracket multi-SMA can be installed in any PC as described in Section 3.5.

At the receiver side, this connection is made through the dedicated ETC card connected to each receiver as described in Sections 3-2 and 3-3. Each receiver with its dedicated ETC card is typically installed in a separate PC.

The **CLOCK CABLES** (described in Sections 2.3.4 and 2.3.9) **must be used** for the CLOCK interconnection. Each CLOCK CABLE has the type and length specified on its sticker as shown in the Picture 2-20 on the left. All cables used for clock distribution must be of the same type and length. Cables of various types and lengths cannot be used within one coherent group of receivers. For interconnection, **only use the original WiNRADiO SMA CLOCK cables supplied with the Clock Kit** as these are specially matched to be coherent.

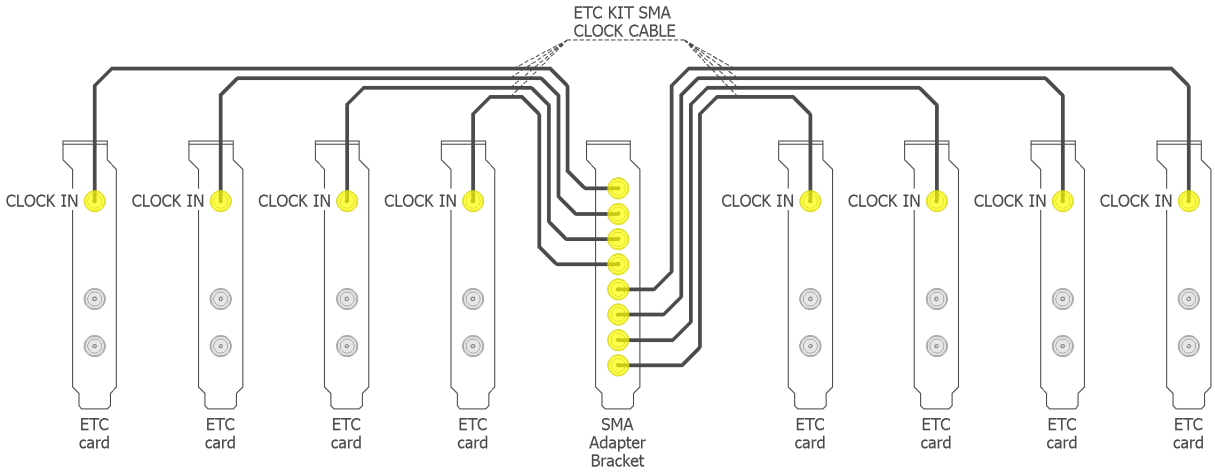
The connection is made in a star-like manner, always linking one of the clock outputs of the Clock Board (through the PCIe Bracket multi-SMA adapter) with one clock input of the receiver on the ETC card connected to it as shown in Picture 3-14.

All receivers within one coherent group are equal from the clock distribution point of view.

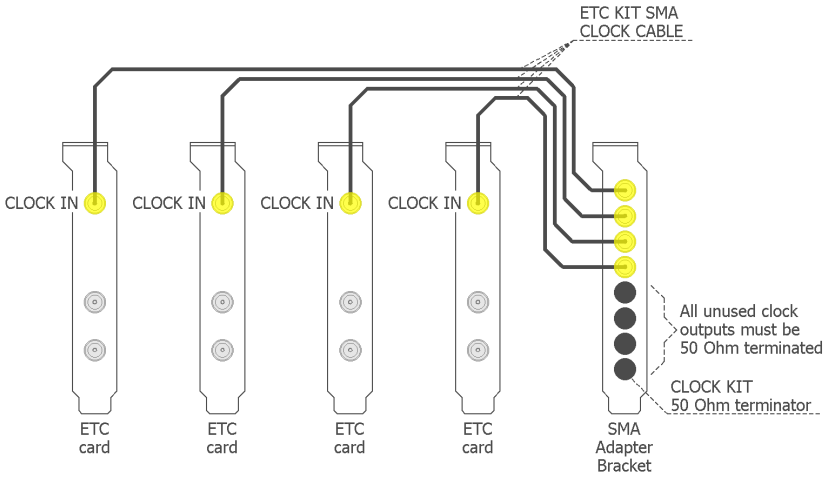
The number of the receivers which can be coherently clocked by one Clock Board is up to eight. Two Clock Boards can be linked for driving up to sixteen receivers as described in Chapter 4. If more than sixteen channels are required, please contact WiNRADiO.

As mentioned above, the **CLOCK CABLES** (described in Sections 2.3.4 and 2.3.9) **must be used** for the CLOCK interconnection. All CLOCK cables used for synchronization must have the same delay specified on them. Cables of various delays cannot be mixed within one coherent group of receivers.

Also please note that the sampling clock interconnects in picture 3-14 are drawn for clarity and there is no need to connect the sampling clock input of any particular receiver to any specific position on the PCIe Bracket multi-SMA Adapter. Instead; all sampling clock outputs on the PCIe Bracket multi-SMA adapter are equivalent. If any of the ports on the PCIe Bracket multi-SMA adapter are unused, all unused ports have to be terminated using the 50 ohm SMA terminators for proper operation (as shown in Picture 3-15). In this picture only four clock outputs are utilized, while the other four unused ports are terminated using 50 ohm terminators.



Picture 3-14: Connecting the sampling clock interconnection. The **CLOCK cables** described in Section 2.3.4 and 2.3.9 **must be used** for the interconnection.



Picture 3-15: When connecting the sampling clock interconnection to less than eight receivers, SMA 50 ohm terminators must be installed on any unused clock output ports.

3.8 Connecting the SYNC interconnection

The SYNC interconnection is made externally, outside the PCs, between the receivers only. This is achieved by using the dedicated ETC card connected to each receiver as described in Sections 3-2 and 3-3. Each receiver along with its dedicated ETC card are typically installed into a separate PC (as a pair).

The **SYNC CABLES** described in Section 2.3.4 and 2.4.9 **must be used** for the SYNC interconnection. Each SYNC CABLE has the delay value specified on its sticker as shown in the Picture 2-20 (on the right). The delay value is marked as “DELAY x CLK” where ‘x’ is an integer number, which specifies the amount of sampling clock periods by which the cable delays the signal. The user must specify the delay of the SYNC CABLE in the software, so that the software can compensate for the delay.

All cables used for synchronization must have the same delay specified on them. Cables of various delays cannot be used within one coherent group of receivers.

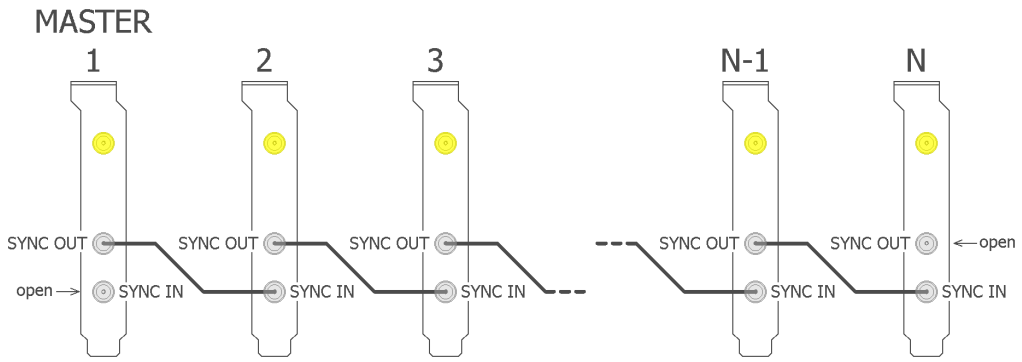
The connection is made in a daisy-chain manner, always linking SYNC OUT of the previous ETC card with the SYNC IN of next ETC card in the chain (as shown in Picture 3-16).

The first receiver in a chain is called the synchronization master and is designated as '1' in the Picture 3-16. The master receiver generates the synchronization signal and sends it down the synchronization chain. Therefore, the SYNC IN connector on the master receiver is left unconnected.

The synchronization signal from the master is received by the receiver second in the synchronization chain designated as '2' in the Picture 3-16. It is received at its SYNC IN input of its ETC card. It is then re-sent through its SYNC OUT output and received by receiver '3' at its SYNC IN input, which also re-sends it through its SYNC OUT to the receiver next in the chain. This way, the synchronization signals propagate down the synchronization chain from receiver-to-receiver, and finally to the receiver which is the last in the chain. The receiver which is the last in chain is designated as 'N' and has its SYNC OUT output left open, as there is no other receiver which could receive the synchronization signal.

The number of the receivers which can be synchronized is unlimited in theory, but currently it is limited to 16 by the software. If more than sixteen channels are required, please contact WiNRADiO.

As mentioned above, the **SYNC CABLES** (described in Section 2.3.4 and 2.3.9). **must be used** for the SYNC interconnection. All SYNC cables used for synchronization must have the same delay specified on them. Cables of various delays cannot be mixed within one coherent group of receivers.



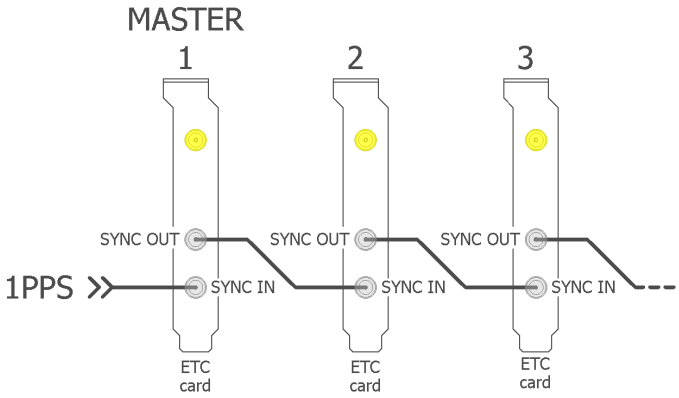
Picture 3-16: The SYNC interconnection is made in a daisy-chain manner, always linking SYNC OUT of the previous ETC card with the SYNC IN of next ETC card. The SMA **SYNC cables** (described in Section 2.3.4 and 2.3.9) **must be used** for the interconnection. The receivers are not shown in the above picture, only the corresponding ETC cards are shown.

3.9 Connecting the 1PPS signal

The 1PPS signal can be connected to the SYNC IN SMA input of the ETC card designated as the master (connected to master receiver), as shown in Picture 3-17. Please note that, the 1PPS signal is not needed for coherent operation of the WR-G35DDCi receivers. The only purpose of the 1PPS signal is to provide a time base for the function of time-stamping. The coherent operation of the receivers is not affected by the 1PPS signal at all.

If the 1PPS signal is not used, the SYNC IN input on the ETC card connected to the master receiver can be left unconnected.

For the technical specification of the SYNC IN input requirements for the 1PPS signal, please refer to chapter 5 of this document.



Picture 3-17: The 1PPS signal can be connected to the SYNC IN SMA input on the ETC card which is connected to master receiver (the receivers are not shown in the picture, only the corresponding ETC cards are).

3.10 Power up and driver installation

Turn on all of the host PCs. Each host PC will recognize each WR-G35DDCi receiver as new hardware connected to it. For installation of the driver and software, please refer to the WR-G35DDCi software installation guide.

4. Extended installation of up to sixteen receivers

To install more than eight and up to sixteen receivers as a single coherent group, two WiNRADiO Coherence Clock & 1PPS Kits (as described in chapter 2.2, the Clock Kits) as well as two PCIe Bracket Multi-SMA Adapters (as described in chapter 2.4) are needed. Two Coherent clock generator boards are interconnected and act as single Coherent clock generator board, providing 16 outputs of the coherent sampling clock.

The two PCIe Bracket Multi-SMA Adapters provide a way for the Coherent clock signals (generated by both Coherent clock generator boards) to be carried out of the PC chassis, so that the sampling clock can be distributed to coherent receivers externally, outside of the PC.

It is strongly recommended that you completely read chapter 3 before continuing to read this chapter. This chapter (4) covers only the differences between the standard and extended installations. It is therefore necessary to perform the installation as described in chapter 3.

4.1 Connecting two Coherent clock generator boards

As mentioned earlier, two Clock Kits are needed to connect from 9 to 16 receivers as a single coherent group of receivers. In such a configuration, one of the Coherent clock generator boards acts as master, the other acts as a slave.

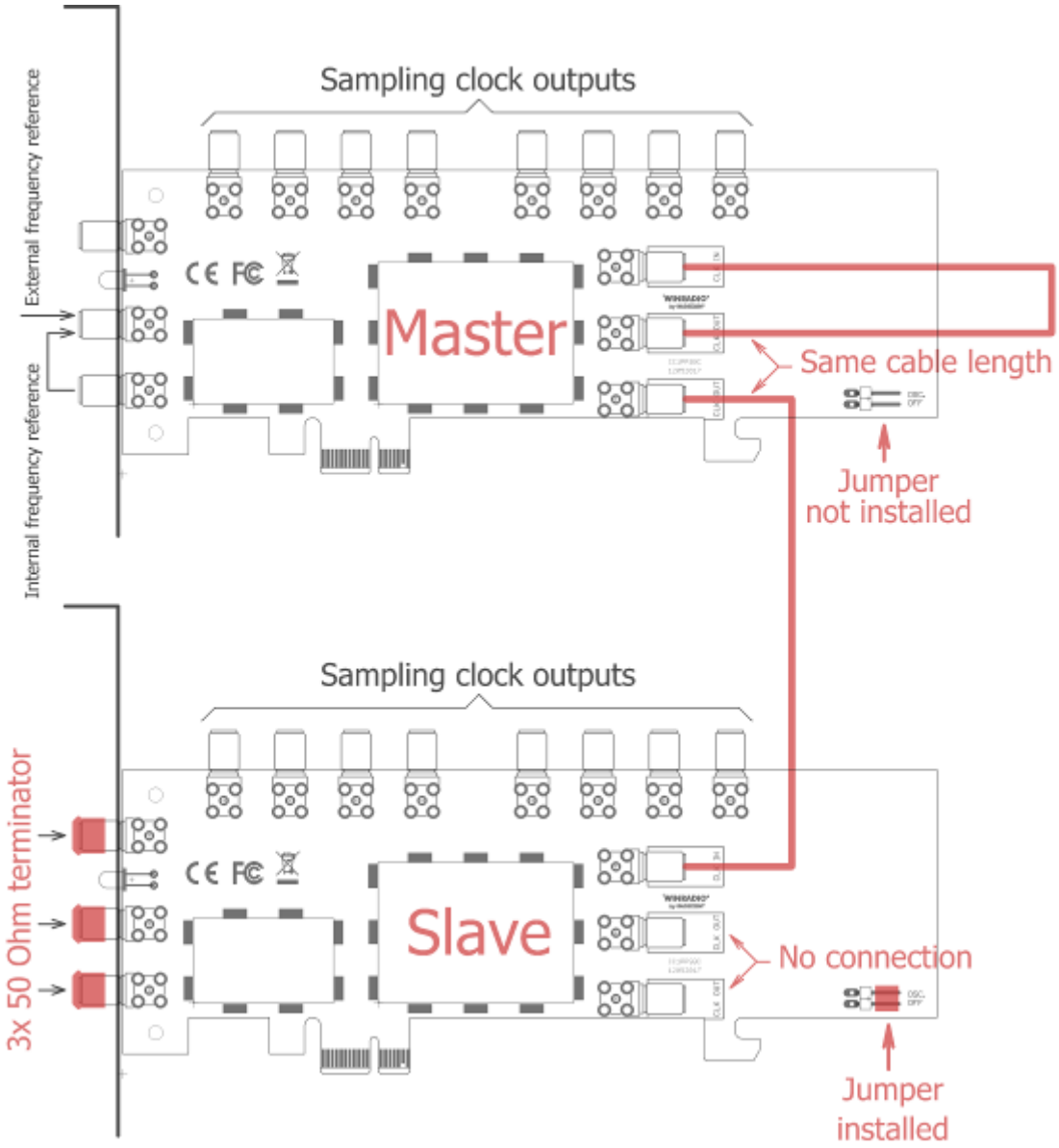
The function of the master Coherent clock generator board is exactly the same as in a single board configuration (as described in 'chapter 3 Installation'). It generates the sampling clock and distributes it to eight receivers. It also generates the frequency reference if an external frequency reference is not used. When using an external frequency reference, connect it to the master Coherent clock generator board only. The 1PPS input and digital synchronization interface is not used and is left unconnected in the ETC configuration.

On the other hand, the function of the slave Coherent clock generator board is solely to distribute the sampling clock to the receivers, the sampling clock is not generated on the slave board. The sampling clock is only generated on the master board and is then fed to the slave board, which then distributes it to the other eight receivers. **The sampling clock oscillator has to be turned off on the slave board to prevent interference**. This is done by installing the jumper onto the pin header used for disabling the sampling clock oscillator. Both the pin header for disabling the sampling clock oscillator and the jumper are described in Section 2.2.16 and shown in pictures 2-13 and 2-14. The installed jumper is shown in picture 4-2.

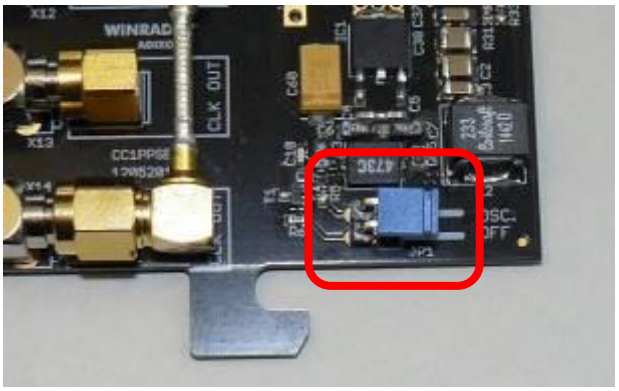
A hook up diagram for two Coherent clock generator boards is shown in Picture 4-1. Use the SMA patch cables for Coherent clock distribution as described in Section 2.2.9 to interconnect both boards. Please note that the same cable as used to interconnect the master and slave boards needs to be used to interconnect the sampling clock output to the sampling clock input on a master board. Also 50 ohm terminators are needed on the slave board frequency reference output, frequency reference input and 1PPS input. The sampling clock oscillator outputs on a slave board can be left unconnected.

Both Coherent Clock Generator Boards have to be interconnected, each with its respective PCIe bracket multi-SMA adapter as described in Section 3.4. Such a connection of sixteen channels is also shown schematically as a part of connection diagram in the Picture 4-3. This way sixteen coherent SMA clock outputs are provided at the rear of the PC where the Clock Boards are installed.

All sixteen sampling clock outputs connected to PCIe Brackets multi-SMA Adapters are equivalent; therefore, any receiver within a coherent group can be connected to any of these SMA connectors on both Adapters. However, any unused ports have to be terminated using the 50 ohm SMA terminators for proper operation as shown in the Picture 3-15.). In this picture only four clock outputs are utilized, while the other four unused ports are terminated using 50 ohm terminators.



Picture 4-1: Interconnecting sampling clocks of two Coherent clock generator boards



Picture 4-2: The jumper for disabling the sampling clock oscillator is installed on the slave board (marked in red). A blue jumper is used for picture clarity.

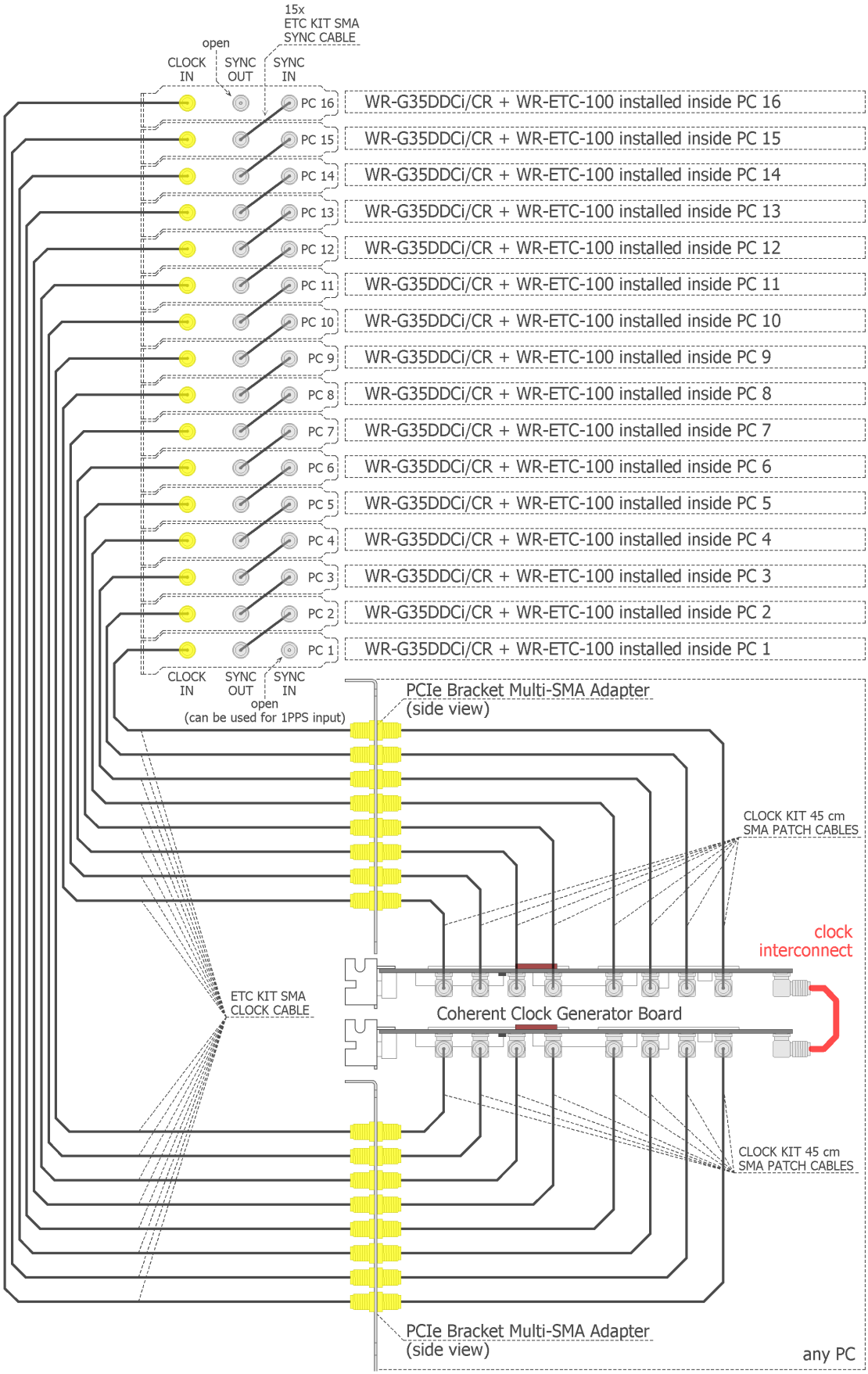
4.2 Installation of receivers

For installation of up to sixteen receivers please refer to Picture 4-3 and Chapter 3 of this document.

Please note that the slave Coherent clock generator only distributes the sampling clock. For the frequency reference input and output, the master Coherent clock generator board must be used. The 1PPS input and digital synchronization interface of both master and slave Clock board are unused in the ETC configuration and have to be left unconnected. For connection of a 1PPS signal please refer to Section 3-9.

Also please note that the sampling clock interconnects in picture 4-3 are drawn for clarity and there is no need to connect the sampling clock input of any particular receiver to any specific position on the PCIe Bracket multi-SMA Adapter. Instead; all sampling clock outputs on both Brackets are equivalent.

If any of the ports on the PCIe Bracket multi-SMA adapter are unused, all unused ports have to be terminated using the 50 ohm SMA terminators for proper operation (as shown in Picture 3-1 and Picture 3-15). Where only four clock outputs are utilized, the other four unused ports are terminated using 50 ohm terminators.



Picture 4-3: Sampling clock and digital sync signal interconnection of sixteen WR-G35DDCi receivers. Clock interconnect (marked in red) is described in Section 4.1.

5. Technical specification

Output sampling frequency	100 MHz
Sampling clock output level	+2 dBm min. into 50 ohm
Number of sampling clock output ports	8
Reference frequency	10 MHz
REF IN input impedance	50 ohm
REF IN input level	+2 dBm min.
REF IN frequency tolerance	+/- 20 ppm
REF OUT output level	+4 dBm typ. into 50 ohm
Internal frequency reference stability	0.5 ppm
1PPS input impedance	50 ohm
1PPS input level L	0 – 0.8 V
1PPS input level H	2.1 V – 5 V

6. Contacts

For more information about our products, please periodically visit our Web site ***www.winradio.com***

If you would like to receive regular information and tips about our products, you are welcome to register on-line using our Web page ***www.winradio.com/subscribe***

If you have any comments, questions or suggestions, please use our general enquiry form at ***www.winradio.com/enquiry***

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